WAVECREST Corporation

Jitter Analysis 101
A Foundation for Jitter Measurements

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Jitter Analysis 101
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Section 1

Fundamentals of Jitter Analysis

Intro to Jitter Testing

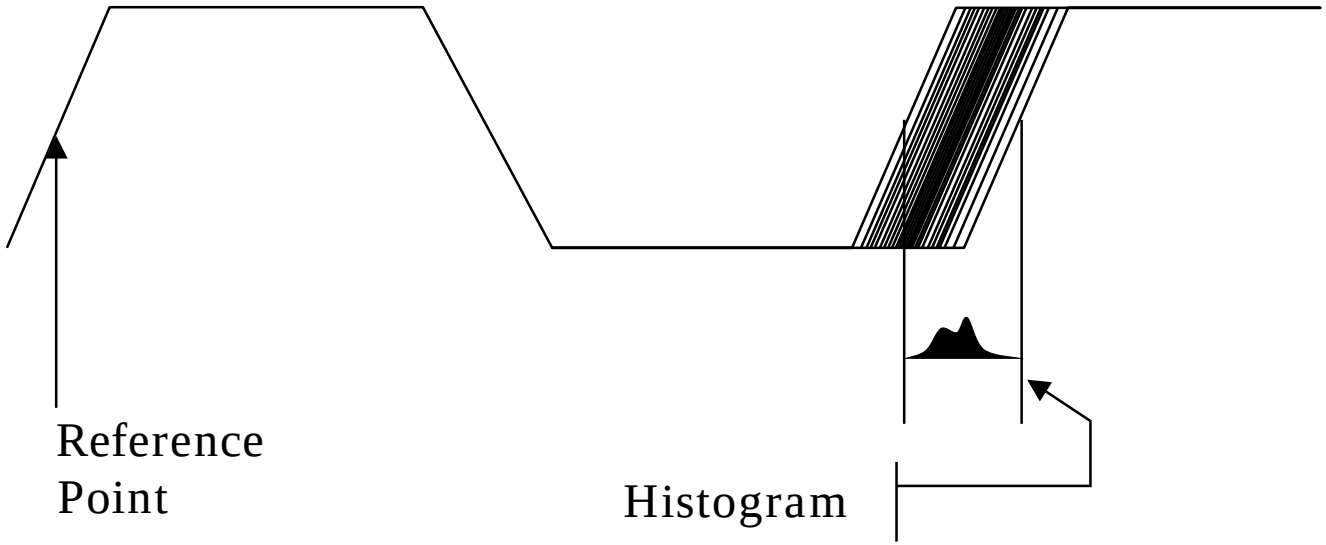
- Why test for Jitter?
  - Device Speeds are exceeding 1GHz
  - Studies show a clear link between jitter and overall device performance and BER
  - For Serial Communications Device Manufacturers, Jitter Testing is faster and more conclusive than production bit error rate testing
    - Fibre Channel specifications call for 14 σ reliability. This would take over 15 minutes to test using a BERT while less than 1 second using jitter techniques.
  - Jitter contributing significantly to timing errors
    - 1 ns of jitter = 10% problem in 100baseT device
    - 1 ns of jitter = 100% problem in Fibre Channel & Gigabit Ethernet devices
  - Jitter can identify process variations.
    - Certain jitter components are sensitive to impurities, thermal variations and cross talk (cross talk may indicate poor insulation layer quality.)
  - Jitter measurements can used to predict the overall reliability of your signal
  - Any others?

What is Jitter?

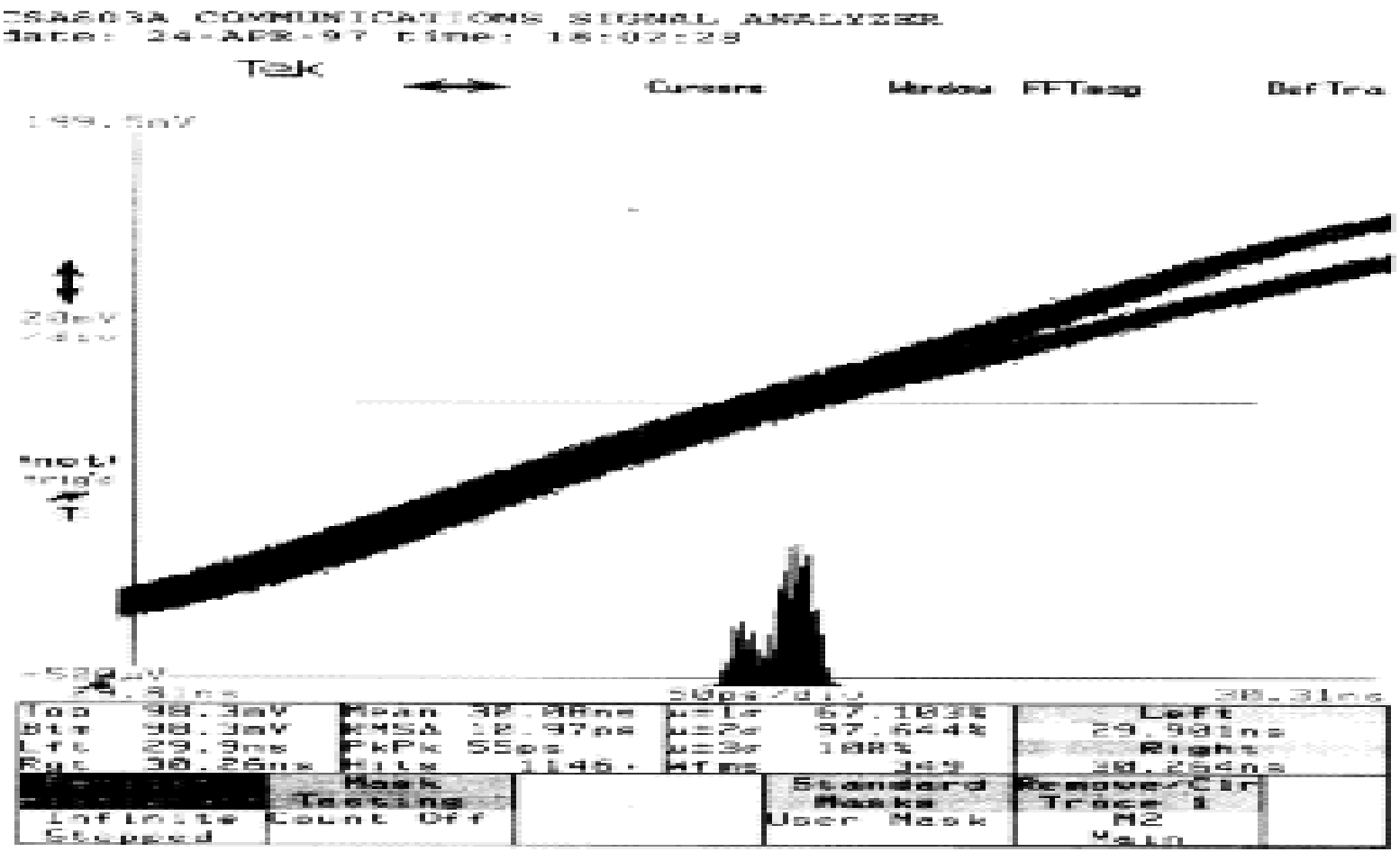
- Jitter -

  "The deviation from the ideal timing of an event. The reference event is the differential zero crossing for electrical signals and the nominal receiver threshold power level for optical systems. Jitter is composed of both deterministic and Gaussian (random) content."

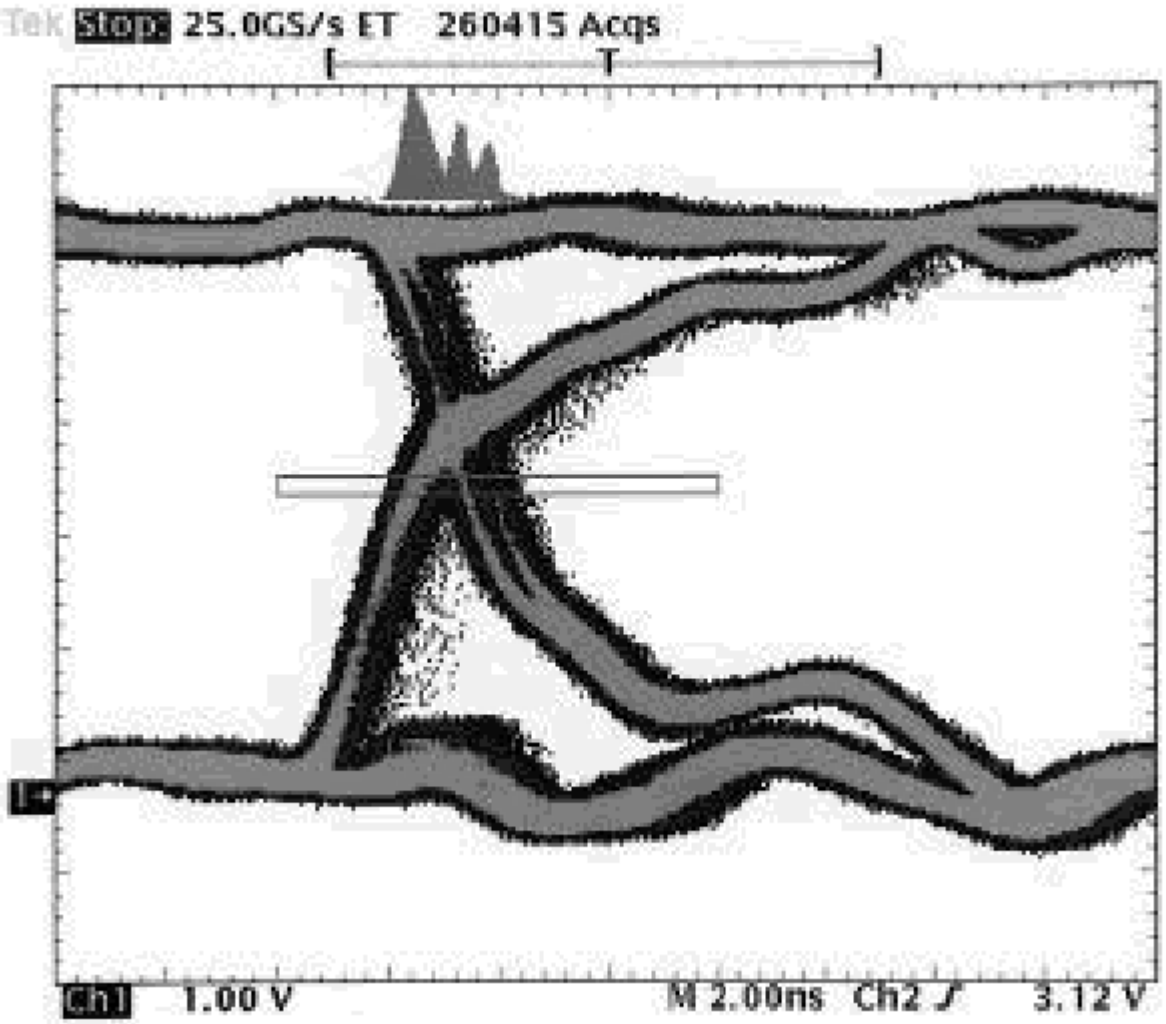
  T11.2 / Project 1230/ Rev 10 Fibre Channel - Methodologies for Jitter Specification page 7.



Using a Sampling Oscilloscope

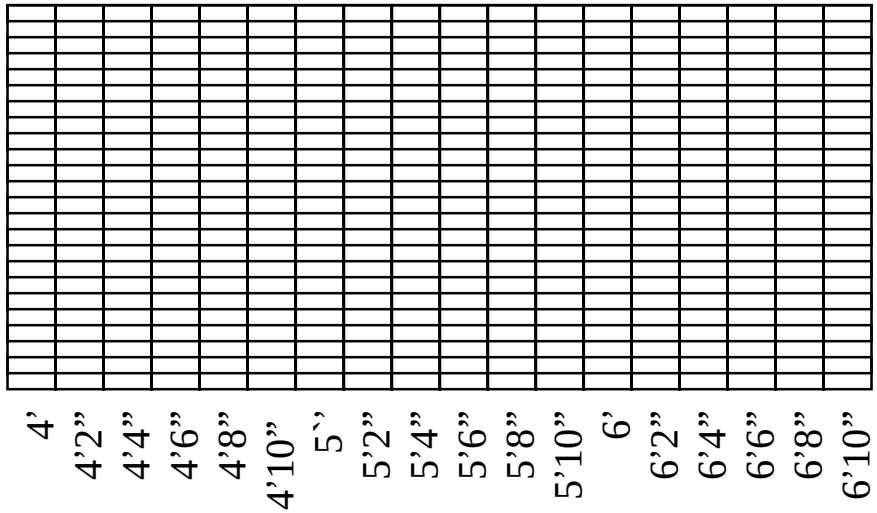


Traditional View Of Jitter



What is a Histogram?

- A Histogram is:
  - A two dimensional plot of the distribution of measurements
    - Each point on the Histogram answers the question: How many measurements had X for a measurement?
  - Compares measurements or data points to the number of occurrences of that particular measurement or data point.
  - A catalog of all measurements made organized by value of measurement.
- An Example
  - Attendees Height



What is Jitter Made of?

Why does it occur?

How will it effect my circuit?

What is Jitter Composed of?

- Deterministic Jitter (DJ)

"Jitter with non-Gaussian probability density function. Deterministic jitter is always bounded in amplitude and has specific causes. Four kinds of deterministic jitter are identified: duty cycle distortion, data dependent, sinusoidal, and uncorrelated (to the data) bounded. DJ is characterized by its bounded, peak-to-peak value."

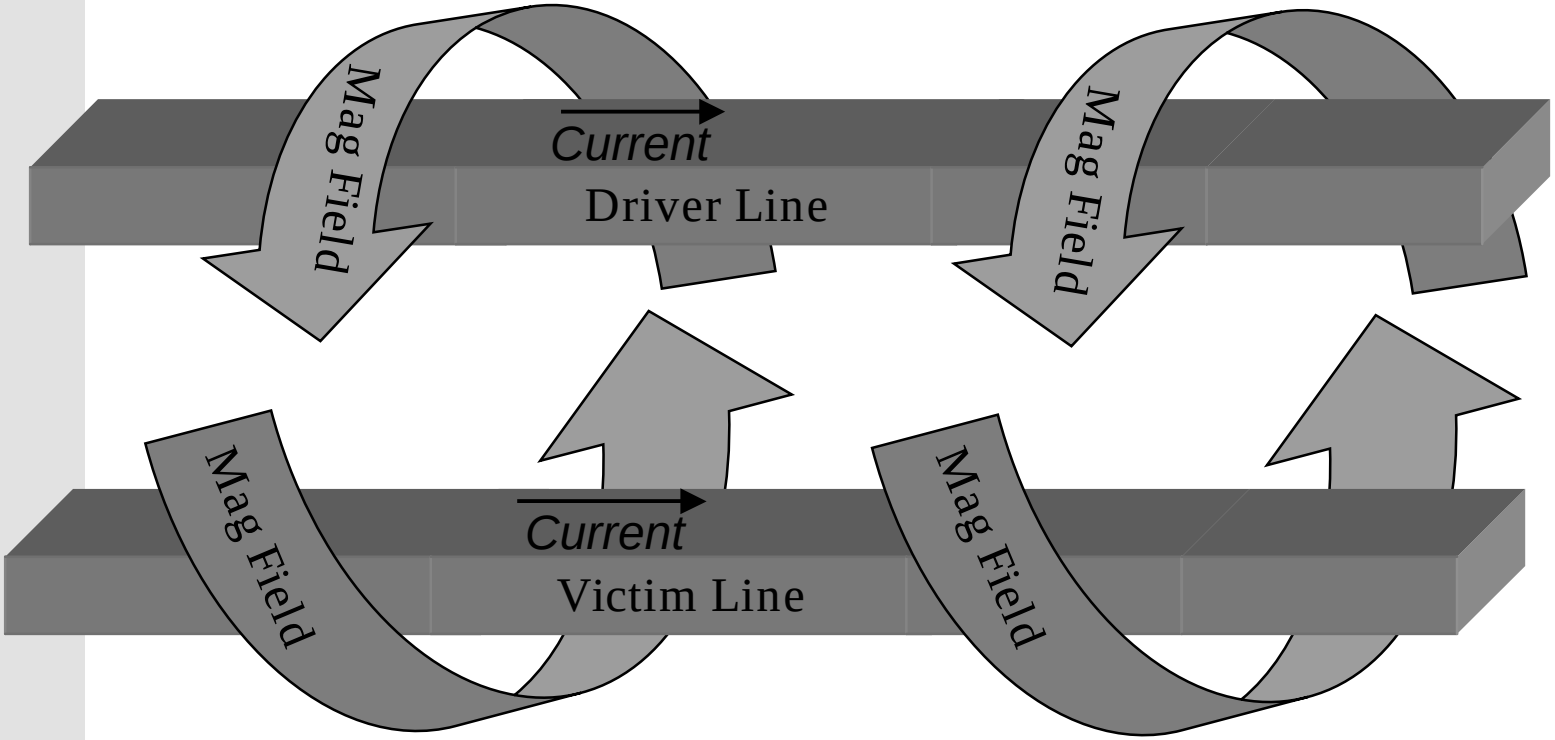
T11.2 / Project 1230/ Rev 10 Fibre Channel - Methodologies for Jitter Specification page 8.

  - DJ will never grow in amplitude regardless of the number of data points such that a sufficient number of data points were taken to complete at least one complete cycle of each periodic element.

  - Clock signals are typically susceptible to Duty Cycle Distortion (DCD) and Periodic Jitter due to cross talk, EMI, Simultaneous Switching Outputs (SSO), device function dependency (pattern dependant jitter)

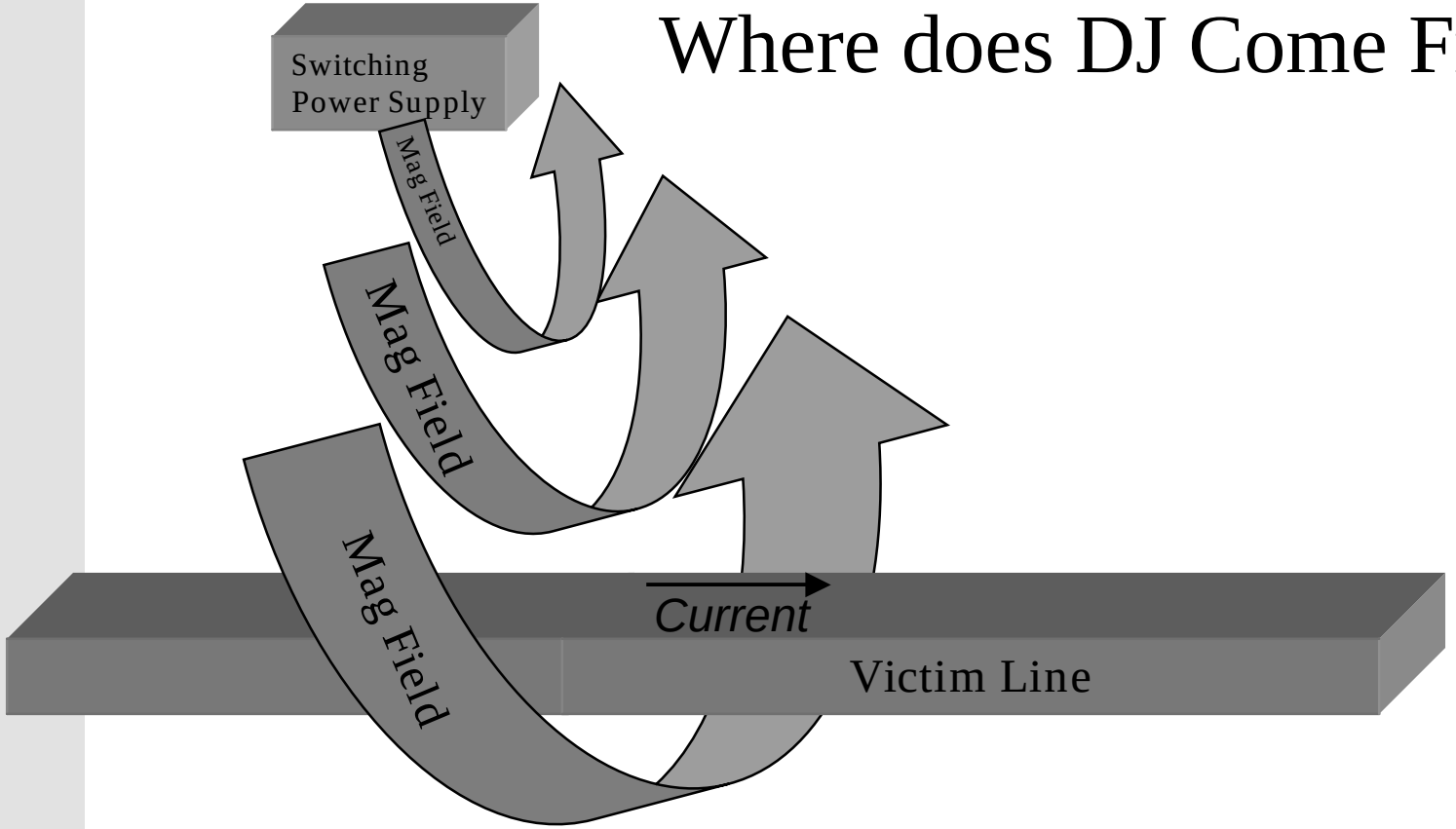
  - Data signals are also susceptible to DCD and PJ as well as Inter-Symbol Interference(ISI) and Data Dependant Jitter (DDJ)

Where does DJ Come From?



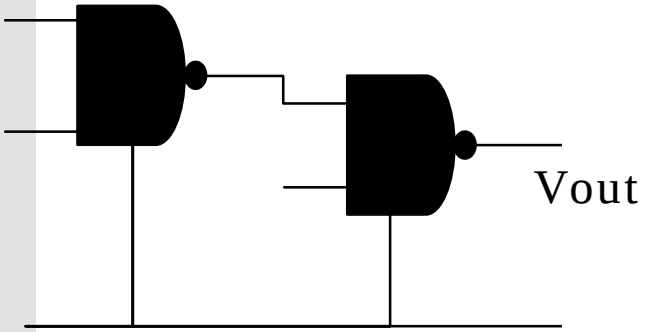
- Periodic Jitter from Cross talk
  - Victim line is affected by magnetic field from Driver line.
  - Incremental inductance of victim conductor converts induced magnetic field into induced current.
  - Induced Current adds (positively or negatively) to Victim Line current increasing or decreasing potential and thus causing jitter on Victim Line

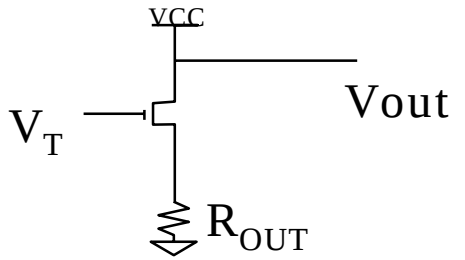
Where does DJ Come From?

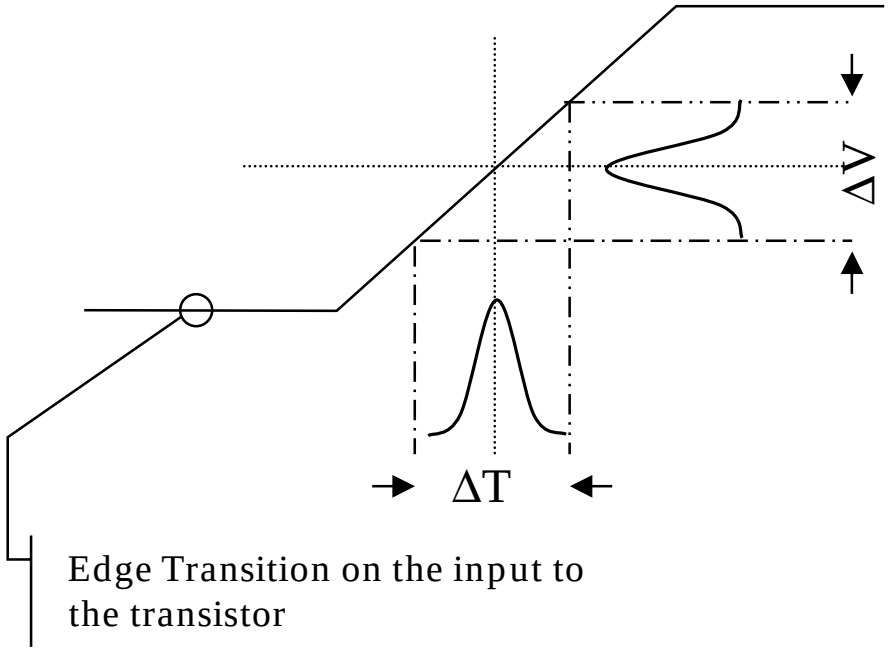


- **EMI Radiation**
  - Victim line is affected by magnetic field from EMI Source. This could be a power supply, AC Power line, RF signal source, etc.
  - As in cross talk induced jitter, the magnetic field induces a current that is added (positively and negatively) to the victim line current thereby effecting the timing of the signal on the victim line.

Where does DJ Come From?

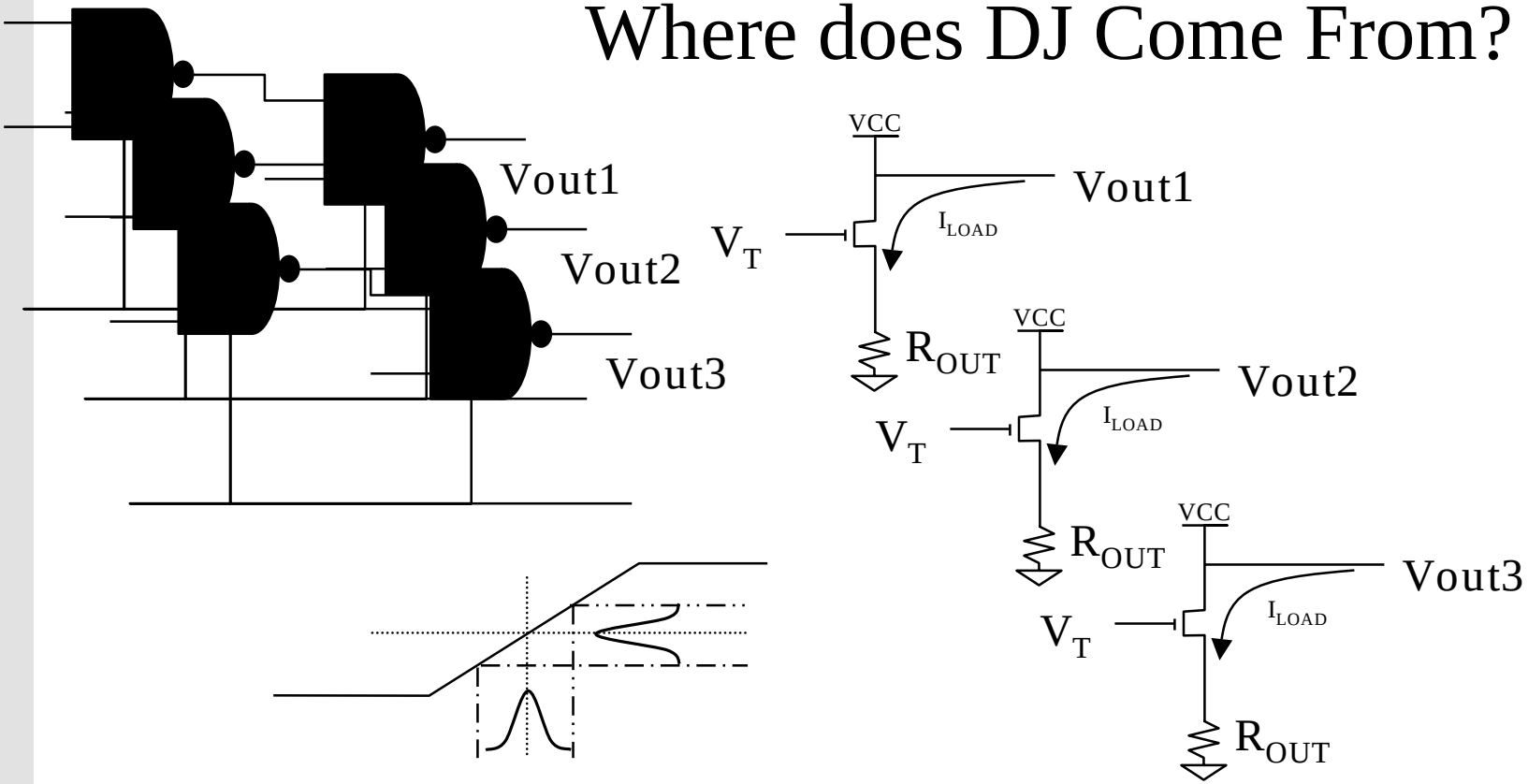






- Noisy reference plane
  - Noise in power planes can result in reference shifts in threshold voltages for downstream logic gates.
  - Resultant timing shift is proportional to slew rate of input signal.
  - The output transistor will switch when V_T is exceeded at the gate.
    - A change in ground reference at V_T will result in a shift in the required voltage to switch the gate thereby delaying or advancing the switch
  - VCO in PLL is sensitive to GND level variance.

Where does DJ Come From?



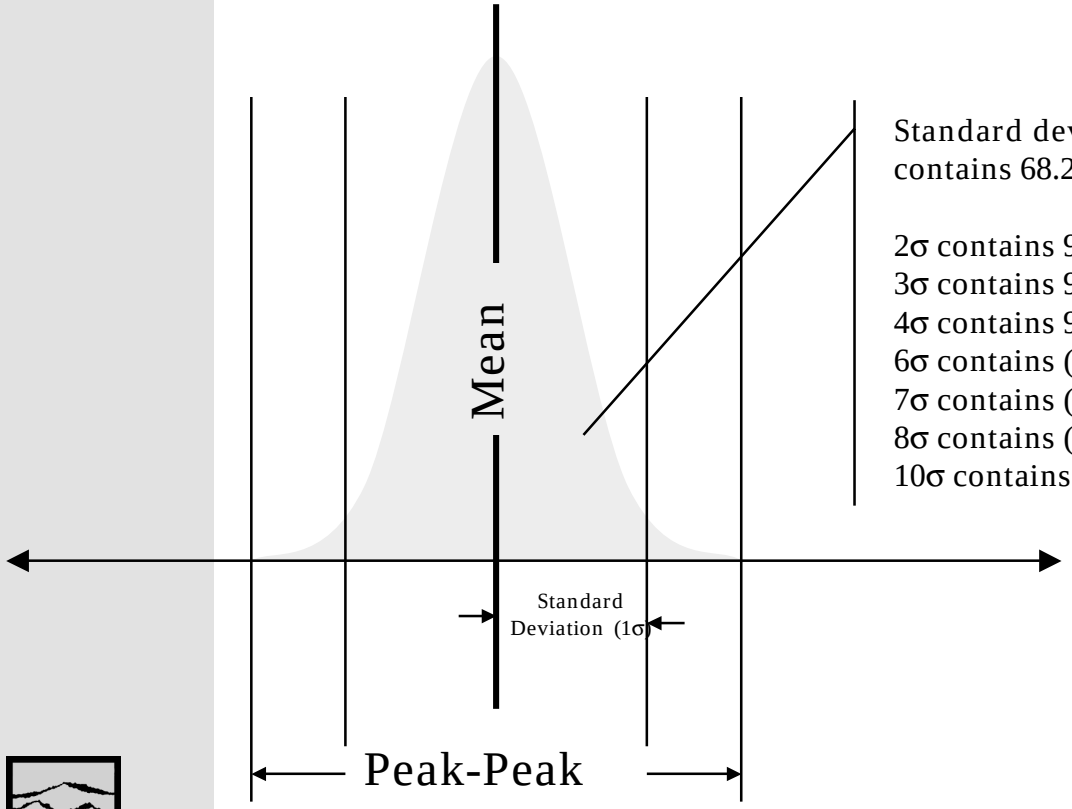
- Simultaneous Switching Outputs
  - If all output pins switch to same state, spike currents will be induced on VCC and on GND.
  - Spike Currents on Reference Plane can cause Threshold Voltage sense point to shift
  - Due to the pattern sensitivity and the bounded max. amplitude of edge jitter due to SSO, this is considered deterministic jitter.

What else is Jitter Composed of?

- Random (Gaussian) Jitter (RJ) -
  - Like all physical phenomena, some level of randomness to edge deviation occurs in all electronic signals. This component is probabilistic in nature and is created by Gaussian noise effects.
  - Random Jitter is unbounded.
- Where does Random Jitter Come from?
  - Thermal vibrations of semiconductor crystal structure causes mobility to vary depending instantaneous temperature of material
  - Material boundaries have less than perfect valence electron mapping.
    - Imperfections due to semi-regular doping density through semiconductor substrate, well and transistor elements,
    - Imperfections due to process anomalies
  - Thermal effects of conductor material. Thermal vibration of conductor atoms effect electron mobility
  - And many more minor contributors such as:
    - cosmic radiation, etc...

What else is Jitter Composed of?

- Random (Gaussian) Jitter (RJ) -
  - Before we can talk about measuring Jitter, it is important to understand Gaussian Distributions as it relates to probability.
- Intro to Gaussian Distributions

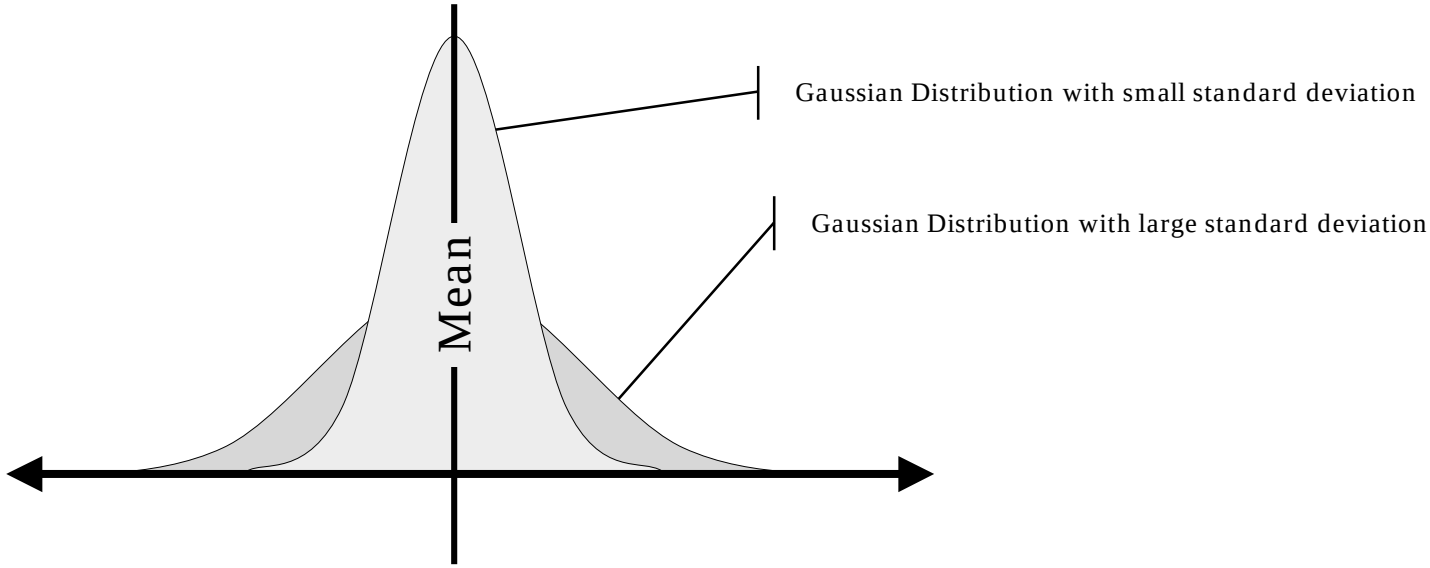


Standard deviation (1σ) is defined as the window in which contains 68.26% of all [measurements] to one side of the mean.

2σ contains 95.4% of all measurements...
3σ contains 99.73% of all measurements...
4σ contains 99.99366% of all measurements...
6σ contains $(100-1.973\times10^{-7})$% of all measurements...
7σ contains $(100-1\times10^{-12})$% of all measurements...
8σ contains $(100-1.244\times10^{-13})$% of all measurements...
10σ contains $(100-1.973\times10^{-21})$% of all measurements...

More Gaussian Statistics

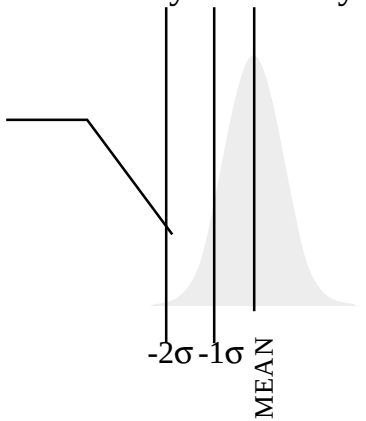
- Gaussian Statistics
  - It is important to note that in pure Gaussian mathematics, all possible measurements are assumed to be possible. However, for all practical purposes, the Gaussian model holds true in electronics for measurement populations not exceeding 10^{21}. This is equivalent to 20σ (single sided).
    - So, go ahead and use these Gaussian assumptions up to a reliability of about 20σ. After that, all bets are off as to the predictability of the measurement. 20s reliability implies compliant operation for at least 321,502.06 years for a 100MHz clock



Why Standard Deviation?

- Standard Deviation is used to predict the occurrence of outlying measurements from the mean.
  - In electronics, it is important to know the frequency of occurrence of edges that are too early.
    - For example, if your system cannot tolerate clock periods that are less than 9.5ns on a 100MHz clock, you would like to know what the probability of a 9.5ns period is. Knowledge of the short period tail can tell you exactly how often a 9.5ns period occurs.

A measurement 2σ away from the mean will have a 95.4% chance of occurring. Thus, once every 250 periods, the period is less than (mean - 2*1σ). If we use the numbers from the previous slide, once every 250 periods the period is less than 9.97ns.



- The Catch…
  - This use of Standard Deviation (1σ) is only valid in pure Gaussian distributions. If any deterministic components exist in the distribution, the use of 1σ for the estimation of probability of occurrence is invalid.

Calculating Standard Deviation

Measurements	
10.2ns	10.2ns
10.8ns	10.3ns
10.6ns	10.5ns
10.2ns	10.2ns
10.3ns	10.8ns
10.5ns	10.6ns

$$\text{Standard Deviation} = \sqrt{\frac{1}{n-1}\sum_{i=1}^{n}(X_i - \overline{X})^2}$$

$$\text{where } \overline{X} = \frac{1}{n}\sum_{i=1}^{n} X_i$$

$$\overline{X} = \frac{1}{12}(10.2+10.8+10.6+10.2+10.3+10.5+10.2+10.3+10.5+10.2+10.8+10.6) = 10.43\text{ns}$$

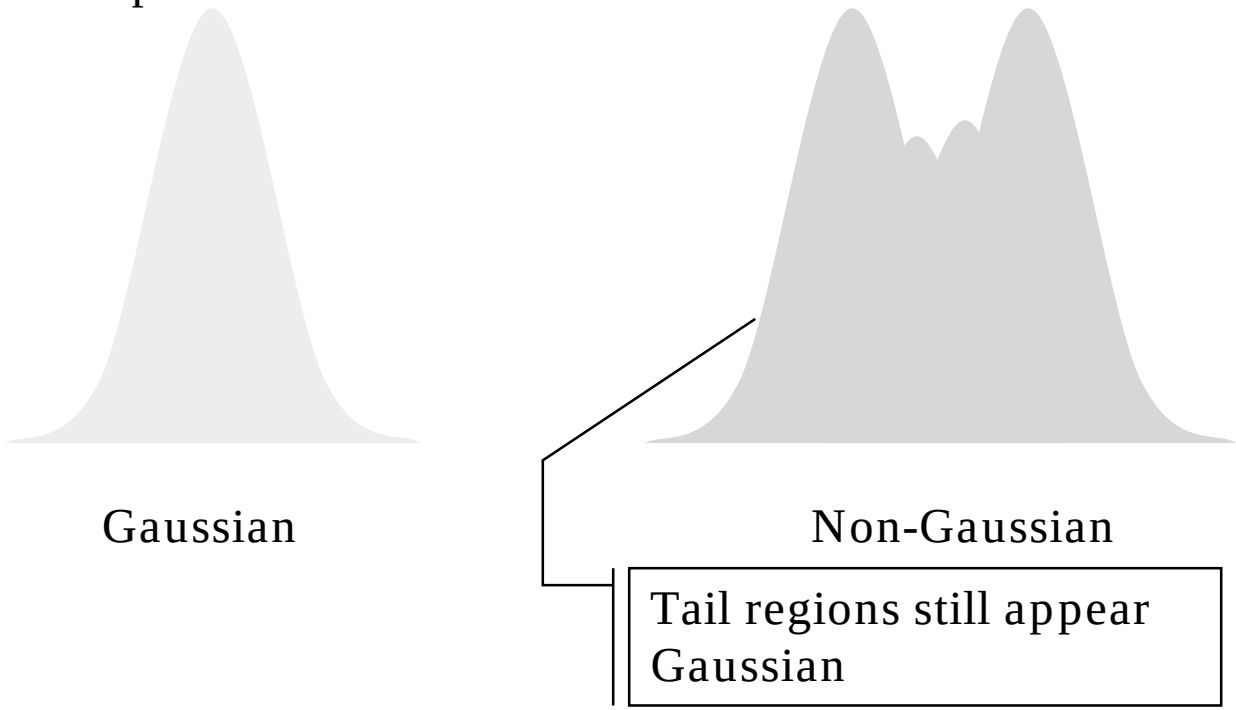
$$\text{Std. Dev.} = \sqrt{\frac{1}{12-1}+\left((10.2-10.43)^2+(10.8-10.43)^2+(10.6-10.43)^2+(10.2-10.43)^2+(10.3-10.43)^2+(10.5-10.43)^2+(10.2-10.43)^2+(10.3-10.43)^2+(10.5-10.43)^2+(10.2-10.43)^2+(10.8-10.43)^2+(10.6-10.43)^2\right)}$$

$$= \sqrt{\frac{1}{11}+(.23)^2+(.37)^2+(.17)^2+(.23)^2+(.13)^2+(.07)^2+(.23)^2+(.13)^2+(.07)^2+(.23)^2+(.37)^2+(.17)^2}$$

$$= \mathbf{.231ns}$$

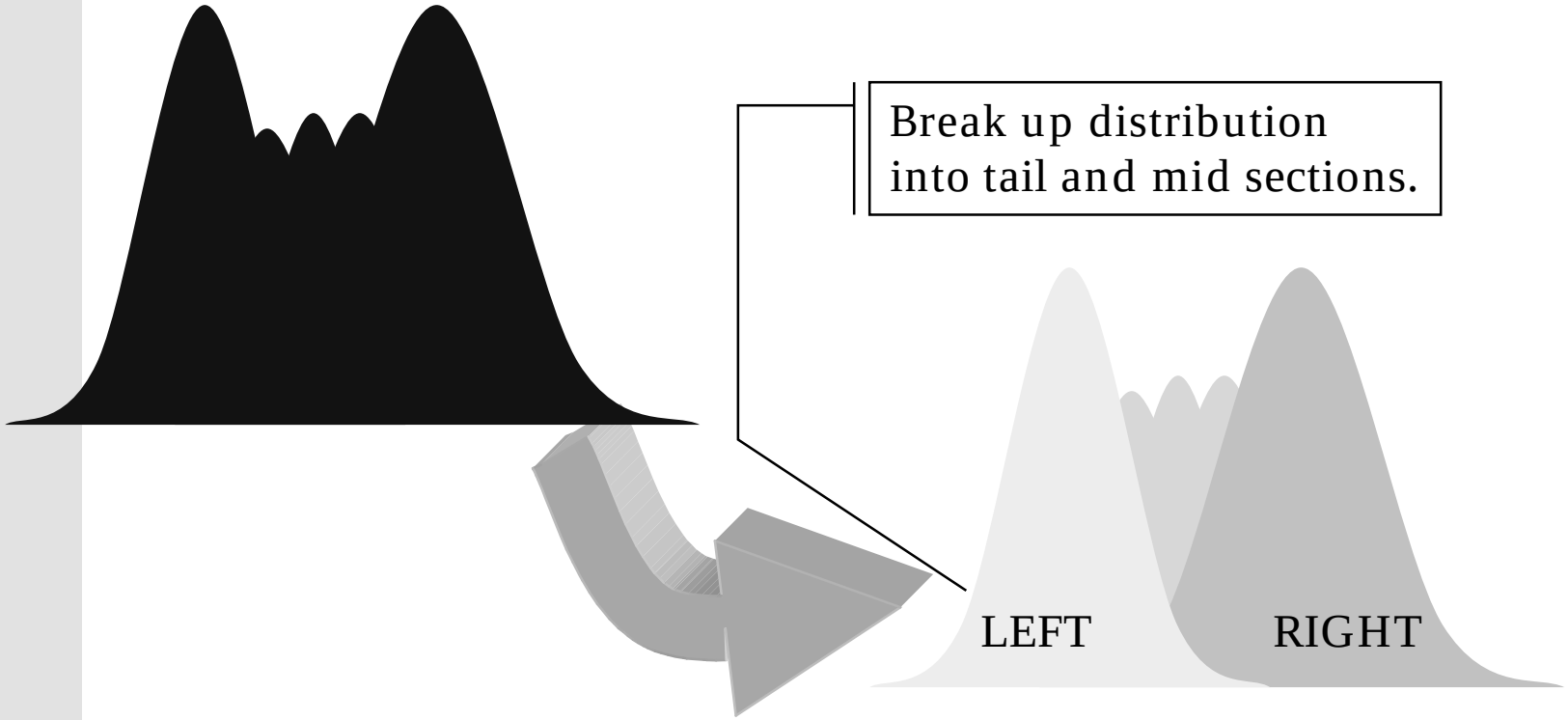
“Real World” Distributions

- In most cases, time measurement distributions are not entirely Gaussian.
  - Typically, some Deterministic/Systematic offset occurs to “mess-up” the distribution to make it Non-Gaussian



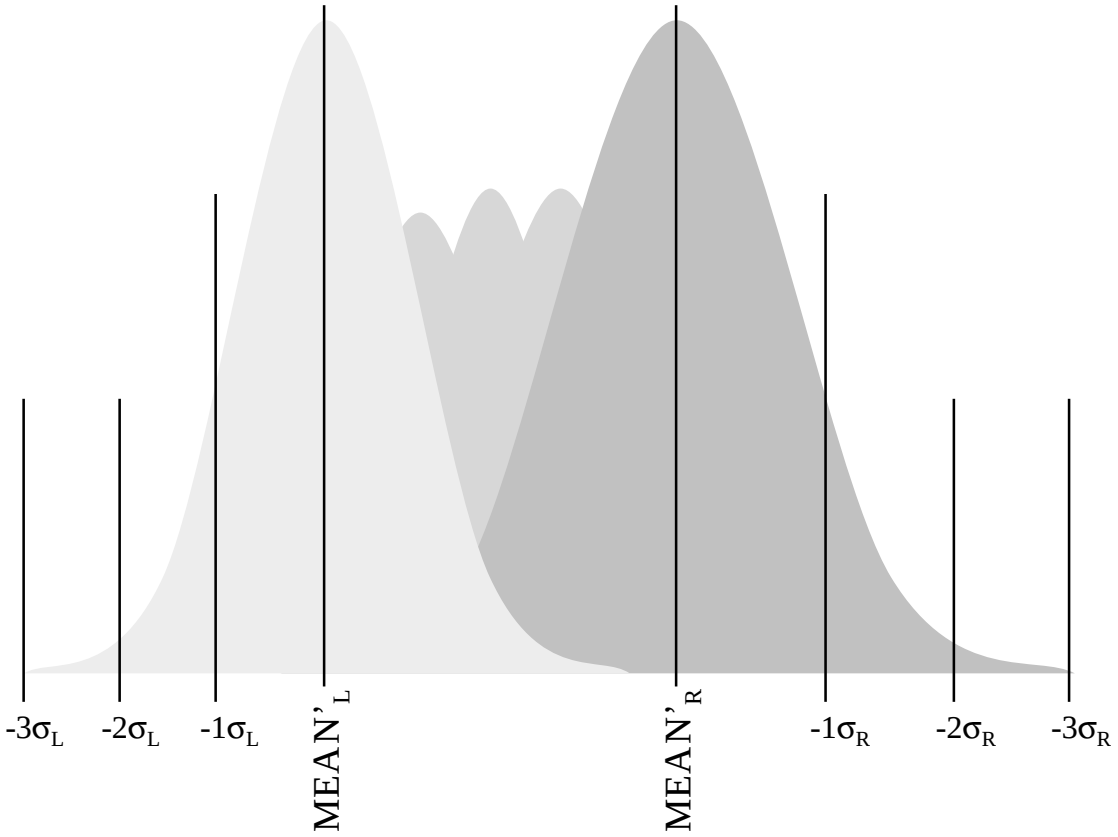
In non-Gaussian distributions, Gaussian assumptions apply to the tails (left most and right most regions) if and only if the equivalent 1σ of these tail region can be calculated.

Non-Gaussian Distributions



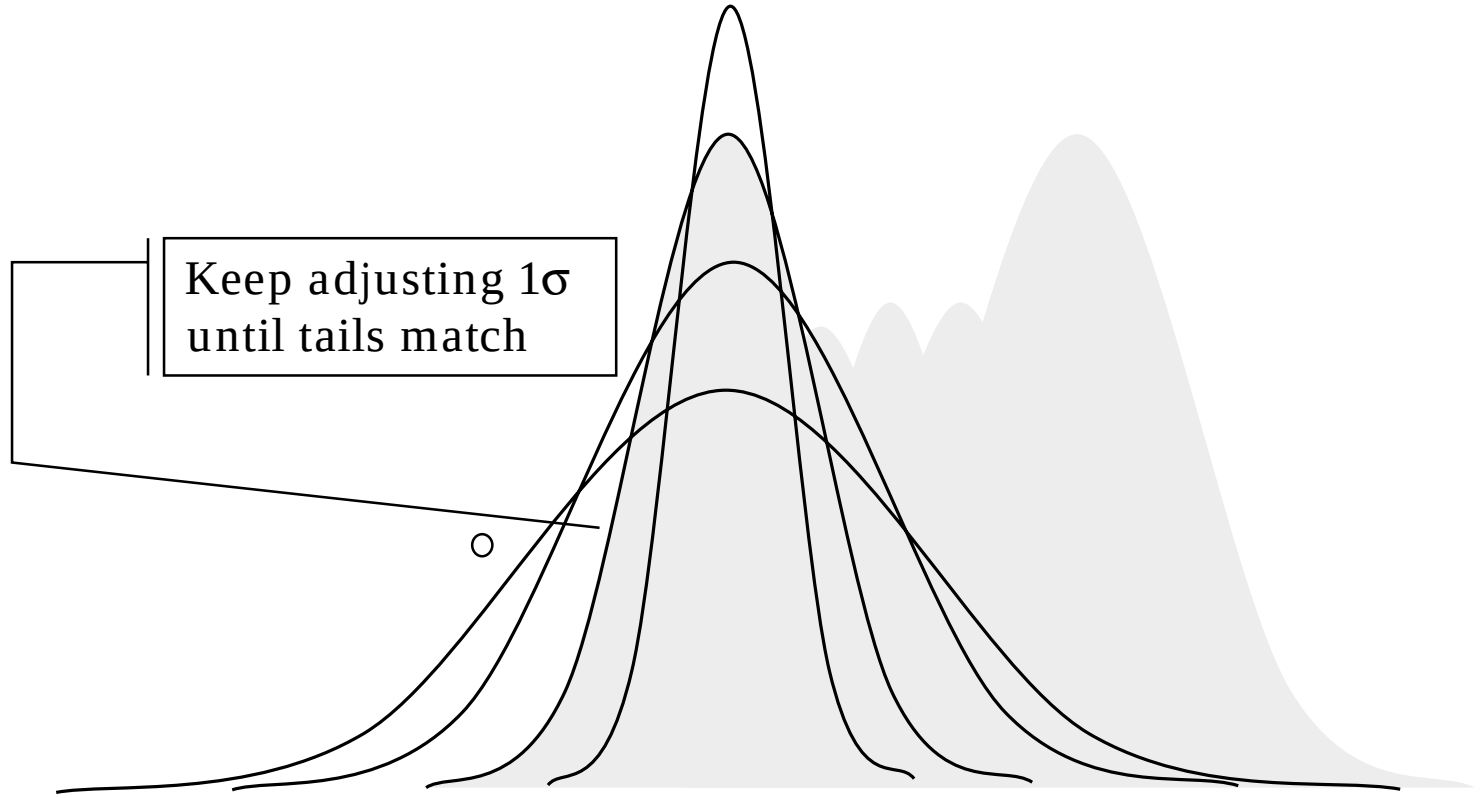
- Analyze distribution by looking at tail sections separately.
  - Allows for probabilistic estimations of out lying measurements
  - knowledge of Gaussian component (Random Jitter) on left side of multimodal distribution enables the calculation of the probability of short cycle measurements.
    - NOTE: Multimodal distributions are those distributions with more than one “hump”. The non-Gaussian example shown here is referred to as bimodal. Some interesting information can be inferred from the shape of this distribution. Symmetric peaks imply equal probability of either mean point (left or right).

Non-Gaussian Distributions



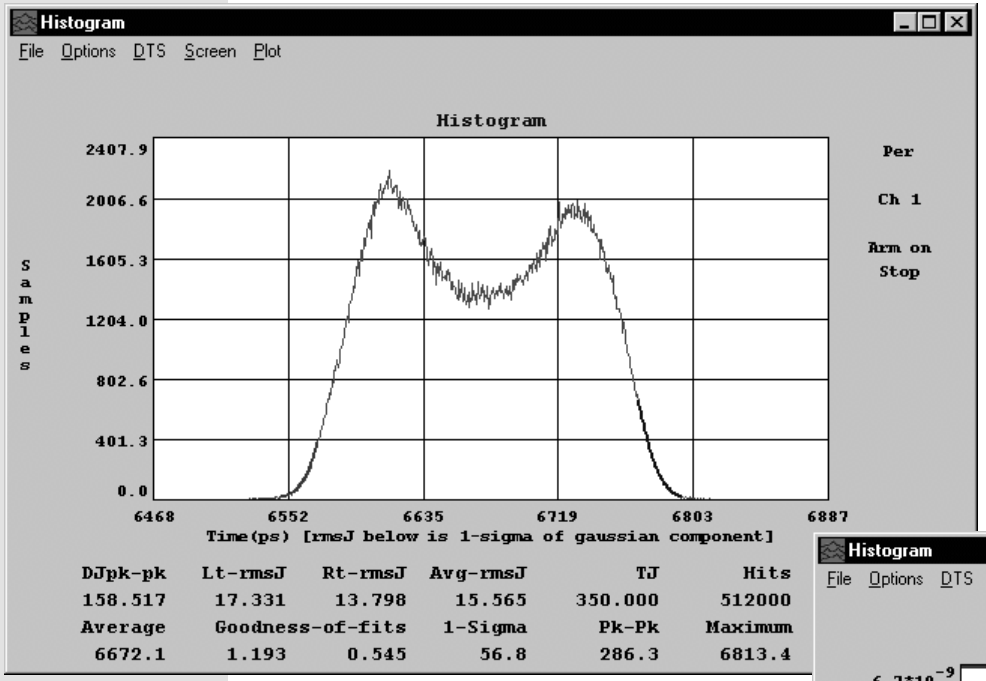
- In order to determine the probability of a measurement occurring at the $-3\sigma_L$ point, it is critical to determine the standard deviation that would correspond to a Gaussian Distribution with a identical tail region to that of our multimodal non Gaussian distribution.
  - Note that the matched Gaussians are not necessarily the same. Either tail can exhibit a larger standard deviation

Determining Representative Gaussian Distributions



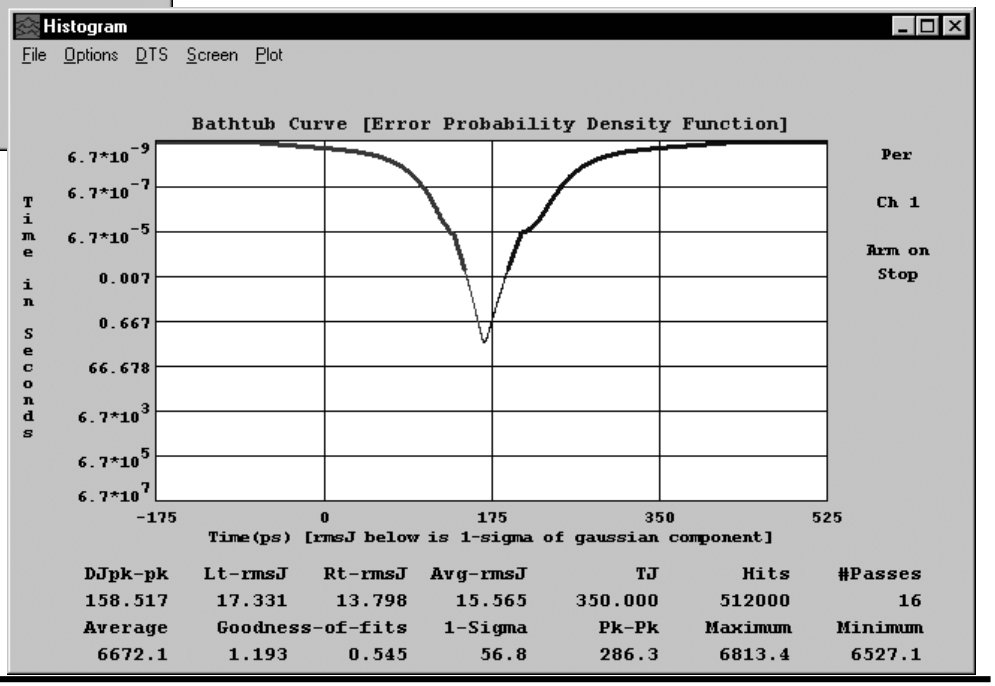
- TailFit™ algorithm enables the user to identify a Gaussian curve with a symmetrical tail region to that of the non-Gaussian distribution under evaluation.
  - Various curves are fitted against the distribution until an optimal match is found. Then, the 1σ of the matched curve is used as the standard deviation multiplier for that particular tail. This is repeated for both sides of the distribution.

An Example of Tail Fit Technique

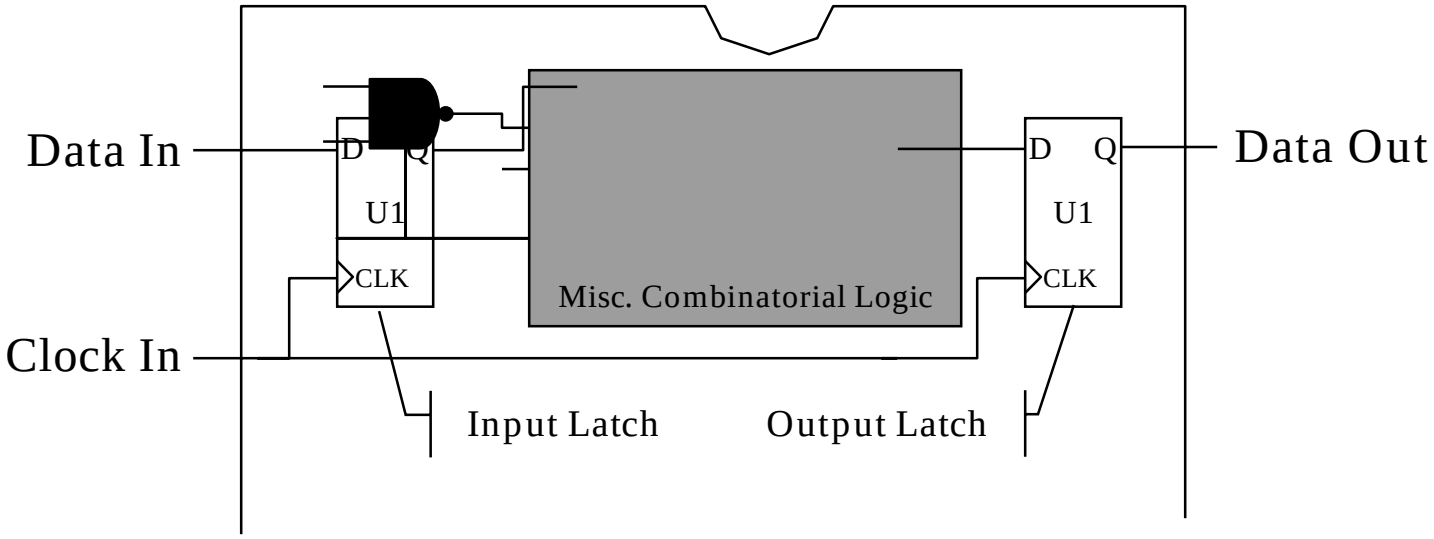


The picture to the left is an example of a distribution with both Random Jitter and Deterministic Jitter. Notice how the Tail Fit curves closely match the tail regions of the distribution.

The $1\sigma_L$ and the $1\sigma_R$ can be used to predict short cycle and long cycle probability. The plot to the left is a PDF plot of period jitter vs spec. This device fails a 550ps jitter spec every 20s of operation.

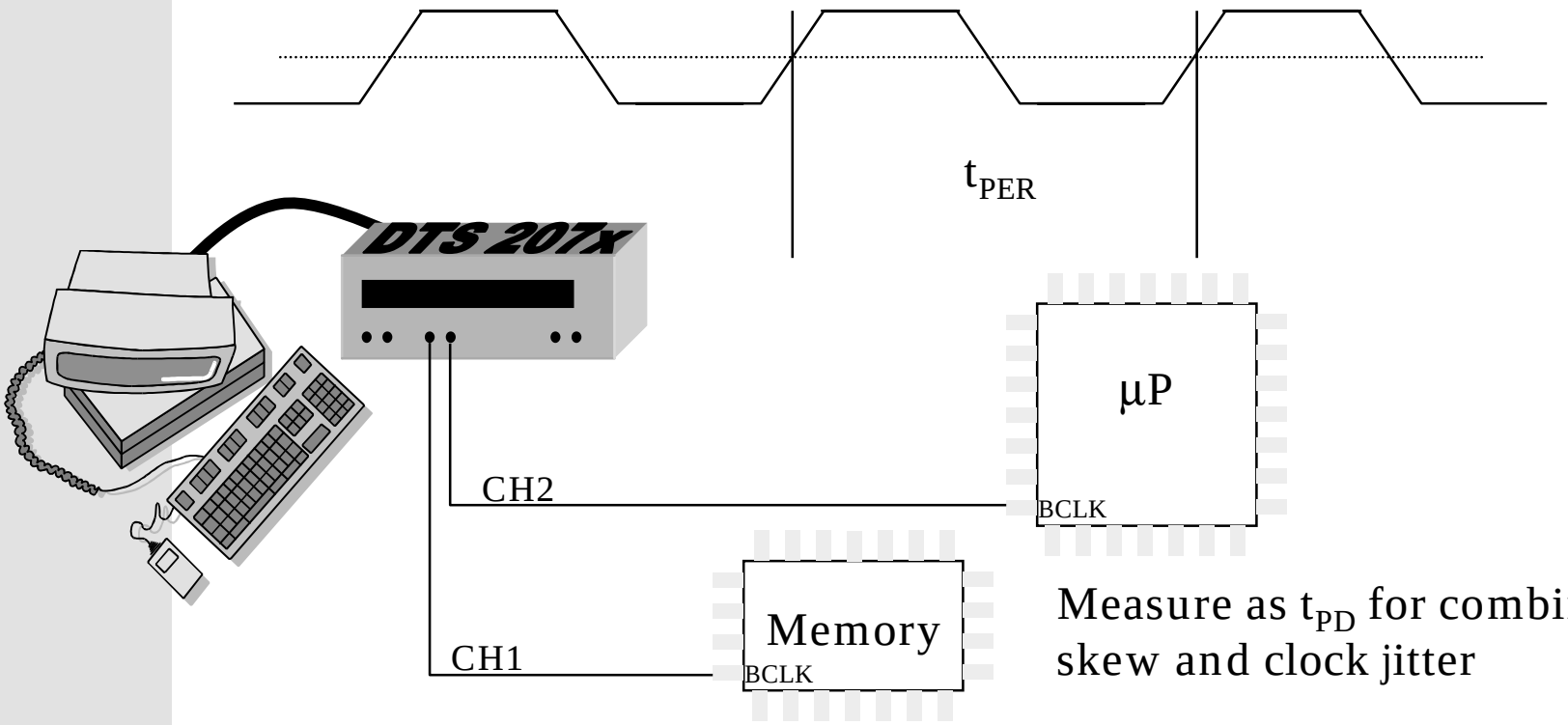


How does Clock Jitter Affect Systems?



- Typical Synchronous Device is susceptible to short cycle errors.
  - This device would latch the wrong data into the output latch if the period was to short. Therefore, the critical measurement for this device is period jitter (rising edge to next adjacent rising edge).
  - This is a typical problem for most synchronous devices and systems.
  - This is sometimes referred to as “Cycle to Cycle”
    - See Appendix for Intel ® Pentium II & III spec and Tektronix application notes for further details

Period Stability (Period Jitter)



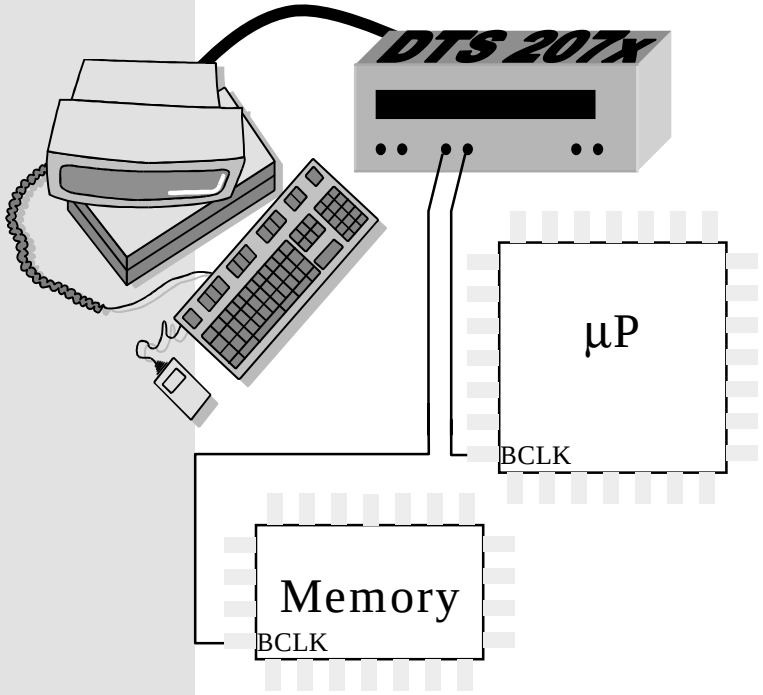
Measure as t_{PD} for combined skew and clock jitter

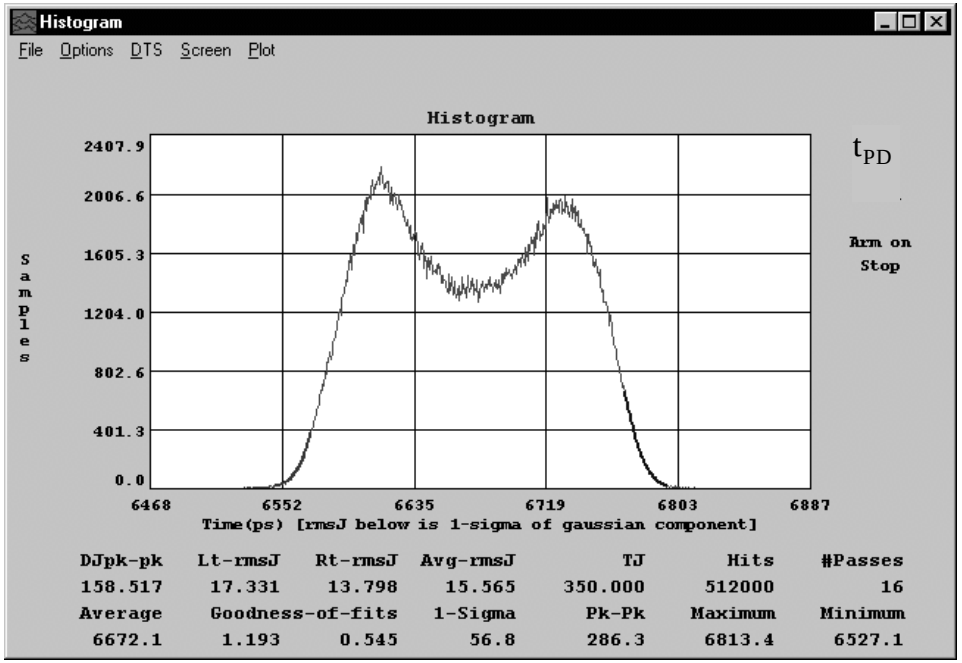
- Intel Period Stability Specification:

  "…should be measured on the rising edges of adjacent BLCKs crossing 1.25V at the processor core pin. The jitter present must be accounted for as a component of BCLK timing skew between devices."

  intel® Pentium® II Datasheet, pg 27

Example Debug Session



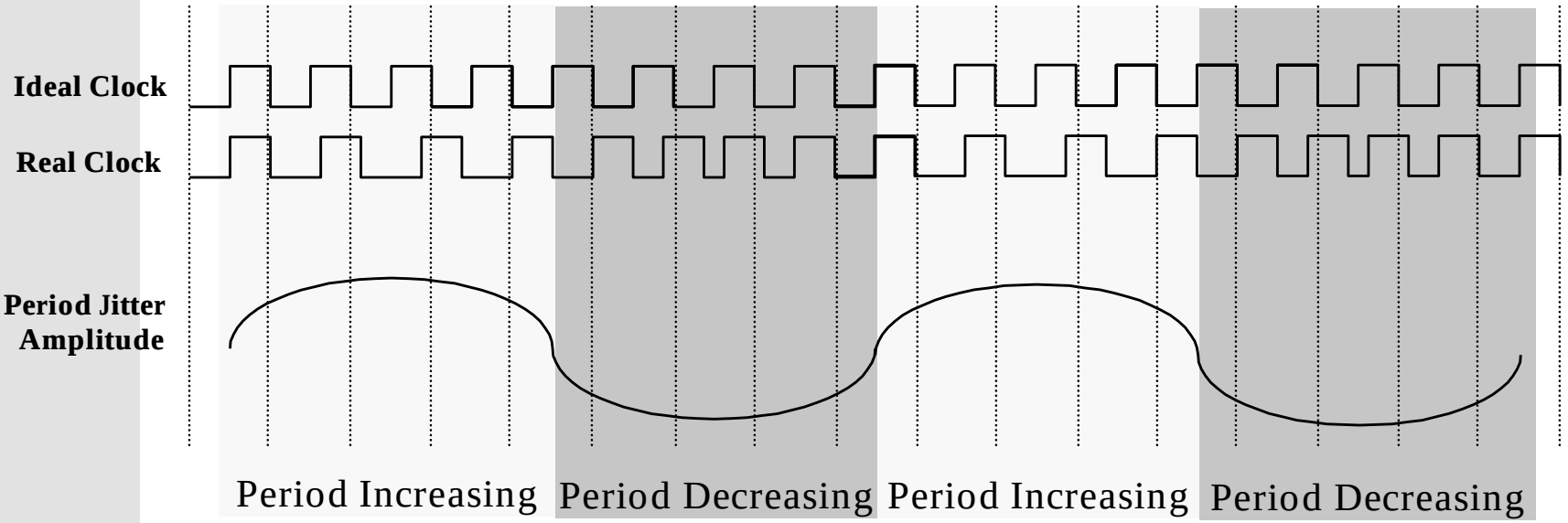


- In this example, note the presence of DJ.
  - The next step would be to determine if the DJ is due to cross talk, pattern dependency, or EMI interference.
  - Use Accumulated Time Analysis to determine Frequency of PJ
  - If PJ is a multiple frequency of clock, use a pattern marker to measure periods relative to the pattern running on the device/system to determine where, if at all, in the pattern the jitter is a maximum.

What is Accumulated Time Analysis™?

- The key to Periodic Jitter Detection.
  - Accumulated Time Analysis is a technique that uses accumulated jitter to determine the presence of periodic jitter.
  - Using ATA, the user can quickly and simply measure the cumulative amplitude and frequency of modulation for all Periodic Jitter elements riding on the clock.
  - Using a patented normalization technique, the user can also see the worst case period deviation due to each of the PJ components.
- What is Cumulative Jitter?
  - Periodic Jitter has the effect of increasing the period and decreasing the period of a clock over time.
    - For example, suppose a clock has a frequency of 100MHz and has a 1MHz Periodic Jitter riding on it which has a peak amplitude of 2ns.
      - The Periodic Jitter will increase the period for 50 consective periods, then, the PJ will decrease the period for 50 consecutive periods.
      - The worst case cumulative period push out occurs after the 50 increasing periods.
      - The worst case cumulative period contraction occurs after the 50 decreasing periods.
      - If the user measures the time elapsed for a random sample of 50 periods, the distribution would be bimodal, and, the time distance between the two peaks would be 2ns. Further, the worst case period push out for a single period would be less than 20ps.

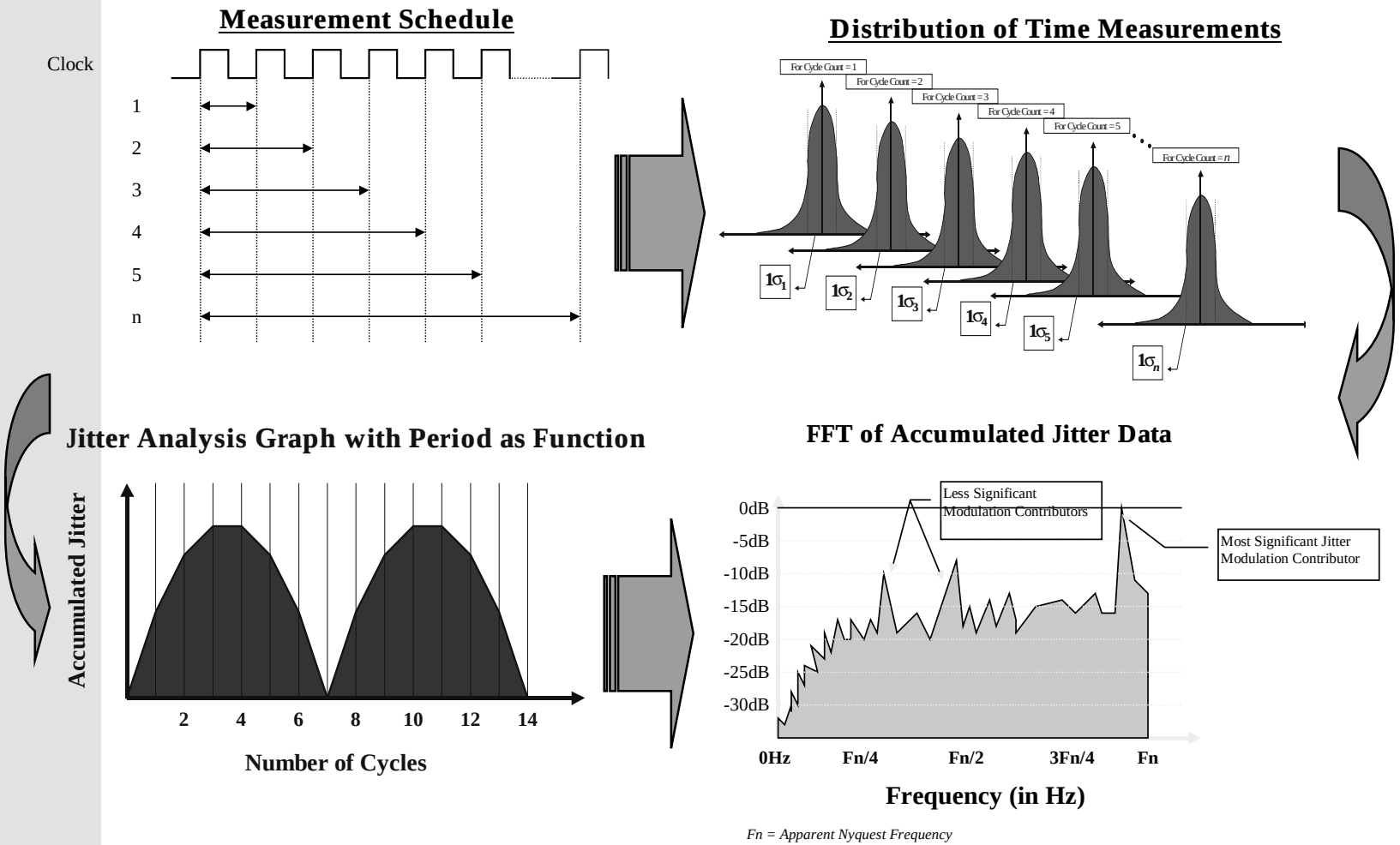
The effect of a Periodic



- Period Increasing
  - In this section the period of the modulated clock is increased from the ideal. Notice how much longer the elapsed time for 5 periods.
- Period Decreasing
  - In this section the period of the modulated clock decreases from the ideal. The net effect of the shorter periods results in a canceling out of the increased periods from the prior section. Note that the same number of clocks is completed after both sections.

It is important to note that the sampling of the waveform must be random so as not to filter any periodic elements.

Accumulated Time Analysis™

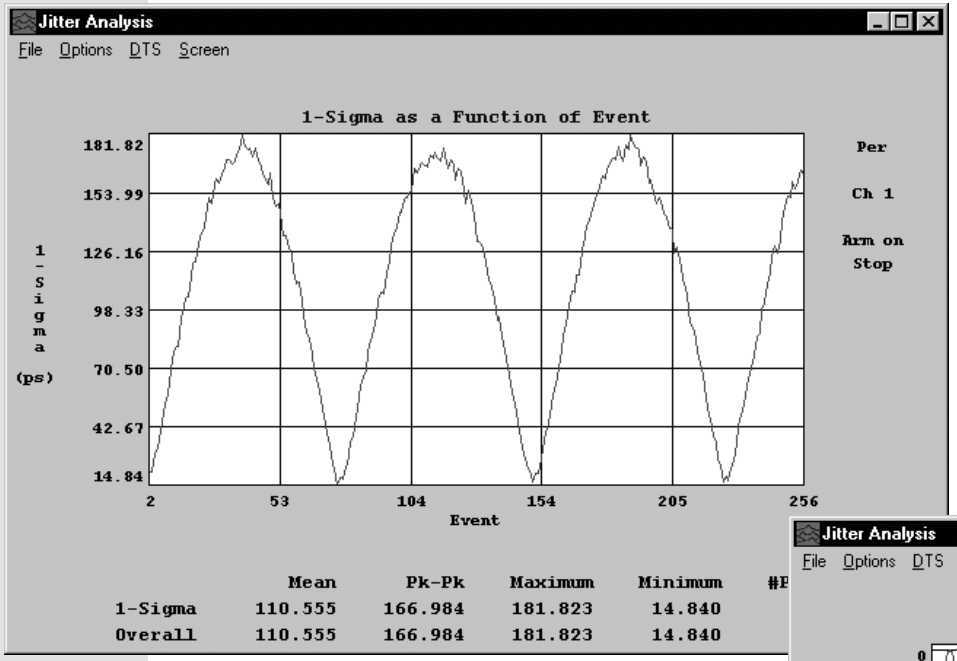


Fn = Apparent Nyquest Frequency

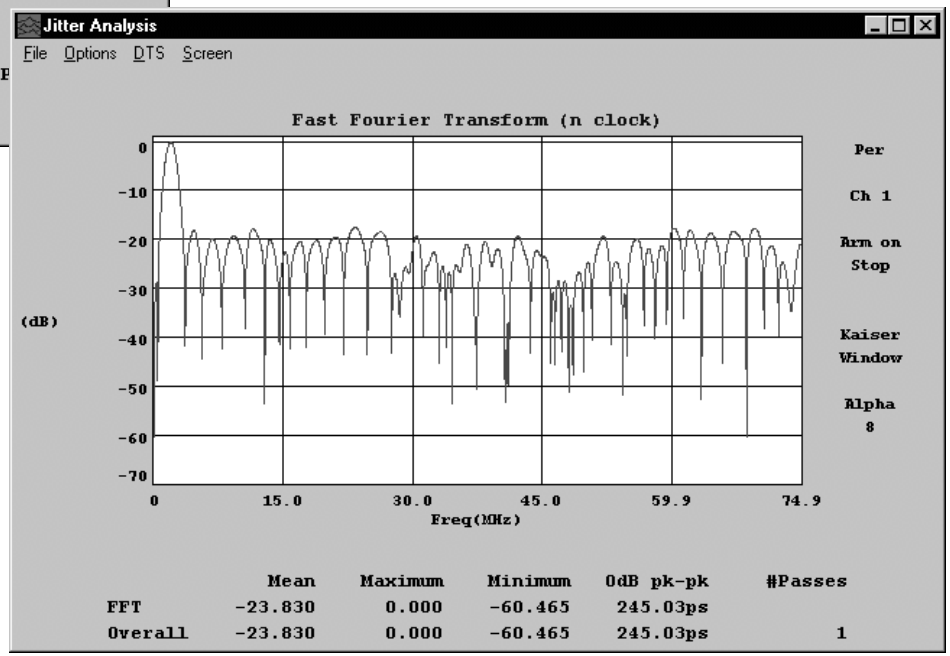
What is an FFT?

- Fast Fourier Transforms (FFT) are used to translate time domain data to Frequency domain data.
  - FFTs are used in oscilloscopes to genenerate a frequency domain plot of the waveform under test.
  - *See Section 4 of this manual for a complete discussion on our implementation of FFT.*
- Wavecrest's FFT of the modulation domain
  - The modulation domain is a plot of the accumulated jitter versus time.
  - The FFT of the modulation domain will show the frequency components of the modulation.
  - Spectral peaks in the FFT of the modulation domain identify Frequency Modulation (FM) components which are riding on the signal under test.
  - The data can be normalized such that the spectral peaks' amplitude will be proportional to it's effect on period jitter.

Using Accumulated Time Analysis



The modulation domain plot to the left indicates a strong periodic with a cumulative jitter amplitude of 101.2ps.

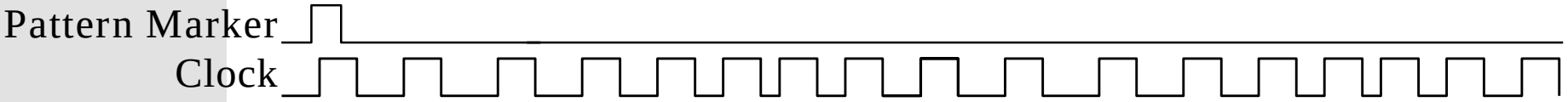


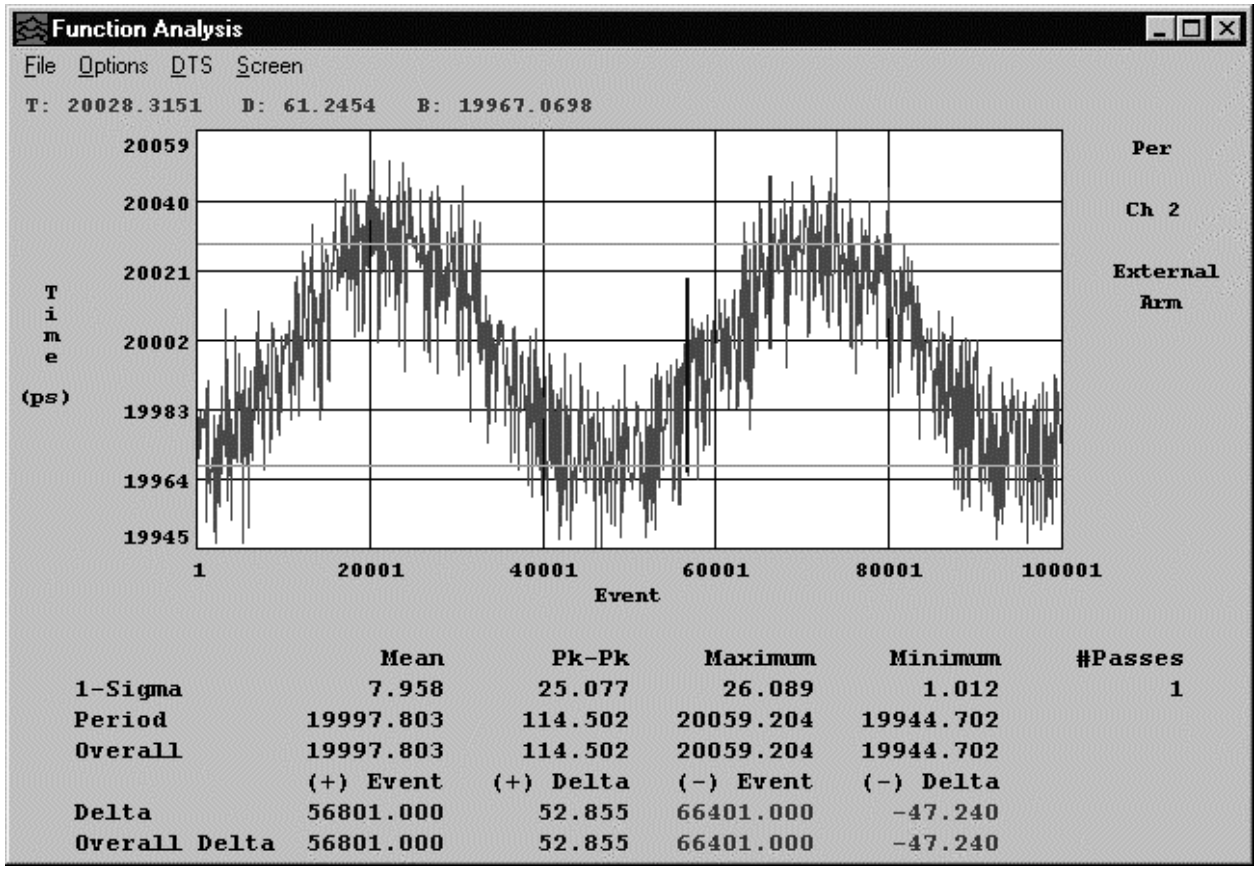
The frequency domain plot to the right indicates a strong periodic at about 1MHz. This tool can also be configured to normalize the peak amplitudes of each periodic element to it's exact effect on a single period. This is called 1-clock normalization.

Pattern Dependant Jitter

- In some cases, the jitter on the clock could be correlated to other electronic activity near by.
  - This could be the case in an imbedded PLL application in which some other circuit in the ASIC is causing the internal PLL to jitter tremendously.
  - In the case of a system design, perhaps another part of the circuit board is emitting an excessive amount of EMI that is interfering with the operation of the PLL or is inducing modulation on the traces distributing the clock signal.
- Debug this using Function Analysis
  - The user can also debug using an oscilloscope and a pattern marker.
    - For sampling oscilloscope, make sure the stability of the reference does not exceed the DJ being diagnosed
    - For real time sampling oscilloscope, make sure the record length completely captures one execution of the pattern.
  - Wavecrest Function Analysis Tool allows the user to look at each and every period after a pattern marker to evaluate pattern dependant jitter.

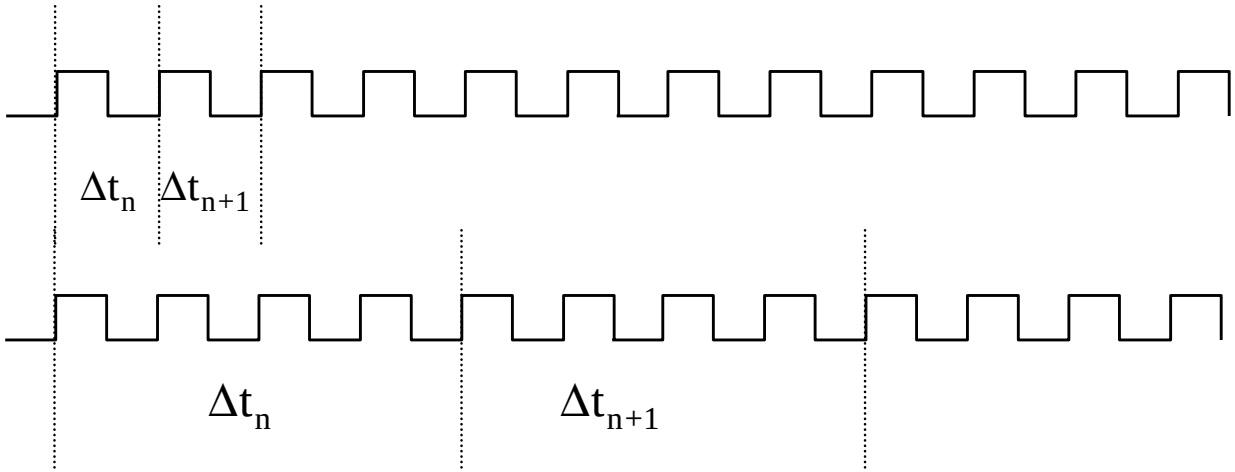
Using Function Analysis





	Mean	Pk-Pk	Maximum	Minimum	#Passes
1-Sigma	7.958	25.077	26.089	1.012	1
Period	19997.803	114.502	20059.204	19944.702	
Overall	19997.803	114.502	20059.204	19944.702	
	(+) Event	(+) Delta	(-) Event	(-) Delta	
Delta	56801.000	52.855	66401.000	-47.240	
Overall Delta	56801.000	52.855	66401.000	-47.240	

Adjacent Cycle Jitter (Rambus Jitter)

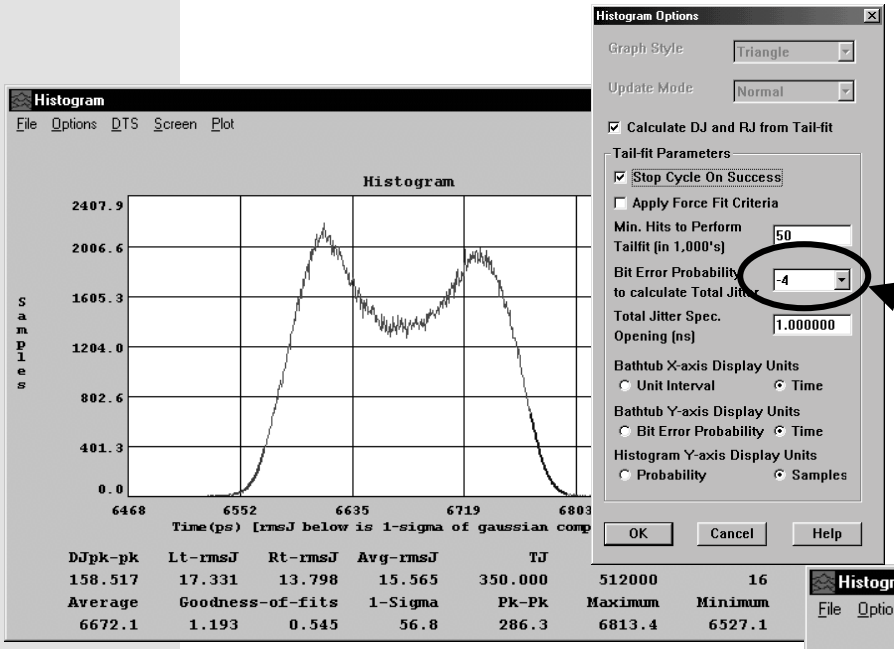


- Adjacent Cycle Jitter
  - Referred to by Rambus as “Cycle-to-Cycle”
    - Since this is inconsistent with established definitions from Tektronix, Intel, Hewlett Packard (Agilent),Wavecrest and many others, we will simply refer to this jitter phenomena as “Adjacent Cycle Jitter”
  - Adjacent Cycle Jitter is the worst case period deviation from one period to the next adjacent cycle. Measurement must be taken at exactly the same voltage for stop as well as start. Rambus requires that 10,000 adjacent periods be analyzed for compliance.

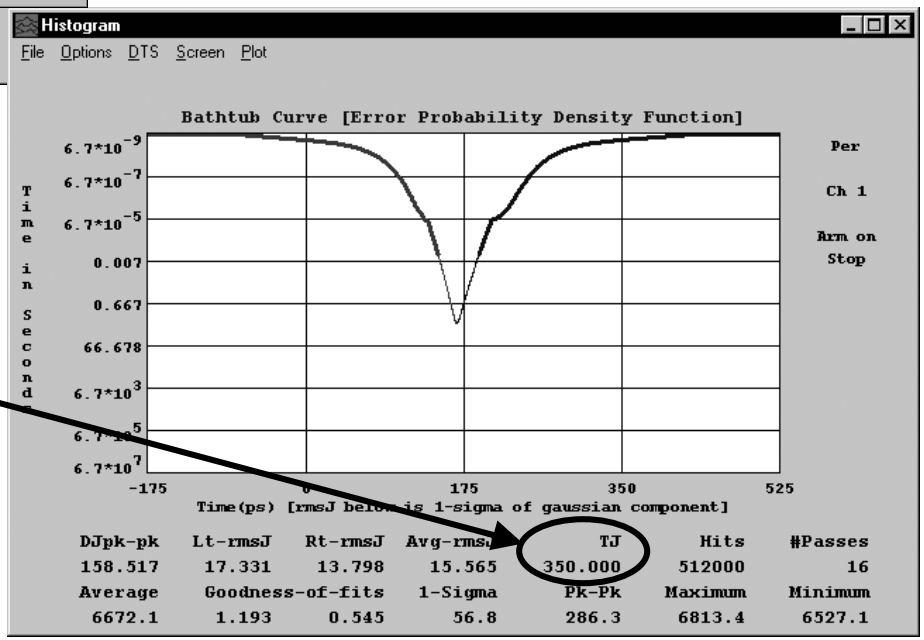
How do you measure Adjacent Cycle Jitter?

- Real Time Oscilloscope.
  - Jitter spec is 50 ps and rise time can be as fast as 160ps.
    - Therefore, for enough samples (3 per edge) on each rising/falling edges, use a real time oscilloscope with a sampling rate of at least 33ps. This is equivalent to a 33GHz Real Time Sampling Oscilloscope.
    - For the accuracy of 50ps, try to get a real time sampling oscilloscope with at least 10x the noise floor and 10x the resolution. So, the ideal real time oscilloscope should have a sampling rate of at least 200GHz.
    - Anything less is a coarse estimate.
- Wavecrest DTS.
  - Wavecrest DTS does not directly measure Adjacent Cycle Jitter.
    - Random Jitter is the overwhelming contributor to worst case Adjacent Cycle Jitter. Therefore, use TailFit to estimate Random Jitter to an error probability of 10^{-4} this is approximately 3σ.
  - Using TailFit™ to estimate TJ for a 3σ reliability is the most accurate way of estimating worst case adjacent cycle jitter over 10,000 adjacent clocks.
    - Deterministic component will automatically be normalized to single period.
    - Random Jitter will be calculated for 10,000 adjacent clocks.

Measuring Adjacent Cycle Jitter

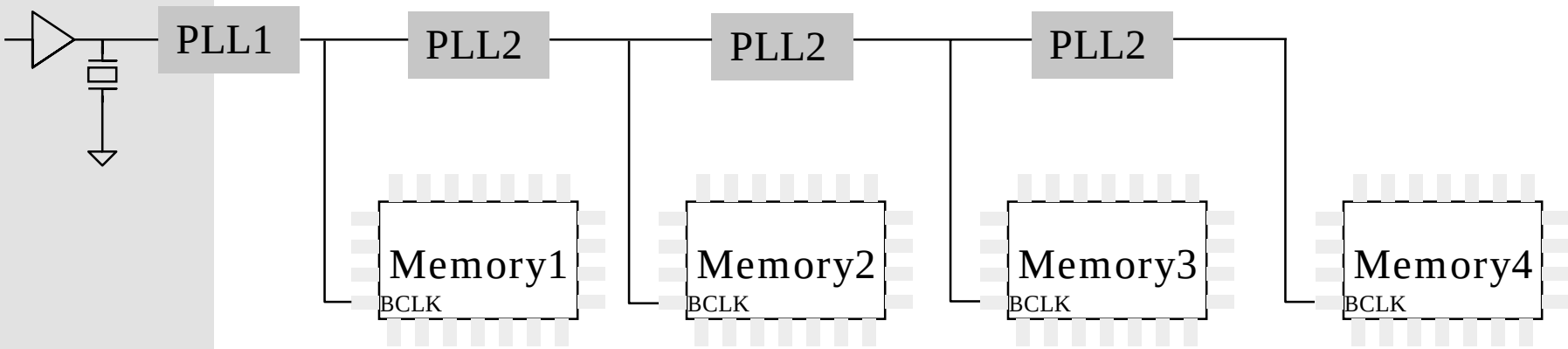


Set Bit Error Probability to (-4) for TJ estimate of 10,000 cycles.



Watch real time effects on TJ while changing other ambient conditions.
Also, note jitter contributors.
Is jitter from DJ, RJ_L or RJ_R?

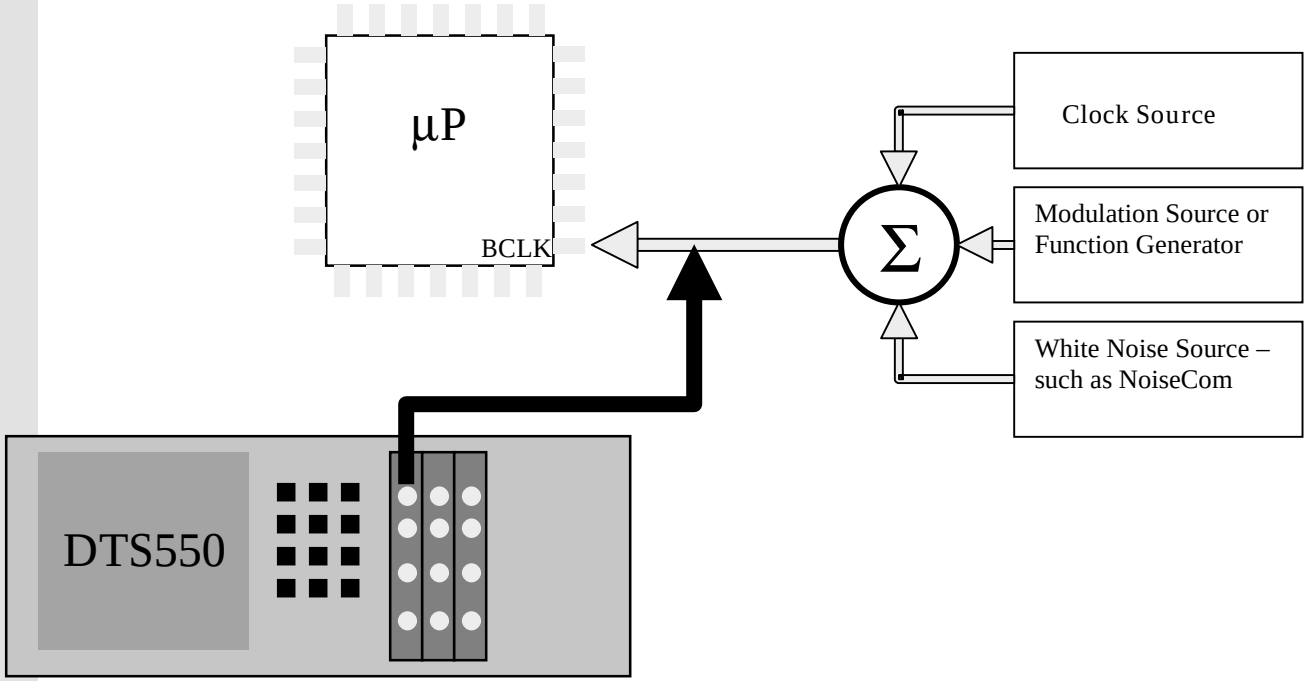
What Happens to Downstream Devices?



- PLL Bandwidth
  - All PLL devices have a cutoff frequency which defines the maximum modulation frequency that PLL can track. Modulation frequencies above the cutoff frequency are simply ignored.
    - So, if EMI radiation of 2MHz were induced after PLL1, and PLL2 has a cutoff frequency of 500kHz, then, Memory 1 will see the modulation on it's clock input while Memory 2 will not.

  (Watch for future Wavecrest tools to measure PLL Bandwidth, loop response, dampening coefficient and much, much more.)
- Jitter Tolerance
  - The downstream devices may be susceptible to many forms of jitter caused by the circuit design, ambient environment or even the PLL driving it. Jitter Tolerance is a measure of how much Jitter a device can handle and still function properly.

Jitter Tolerance In a Digital Network



- Substitute Jitter Generator for PLL signal at each device to test maximum allowable jitter.
  - Can use a series of instruments including a clock source, modulation source and White Noise Source.
  - Can also use Wavecrest DTS550 Jitter Generator for up to 1GHz clock emulation with full jitter programmability.

Jitter Tolerance Testing

- Sweep through frequency range for modulation sensitivity testing.
  - Many internal circuits feature an embedded PLL
  - Since all PLL devices have a bandwidth, it is important to sweep the modulation frequency through several different frequencies to determine specific sensitivities.
- Use several different Jitter combinations.
  - Increase psuedo-random jitter to test for Random Jitter,
  - Sweep Periodic Jitter through several frequencies and amplitudes.
  - Check Power sensitivities to jitter tolerance.
  - Check thermal sensitivities to jitter tolerance.

Section 2

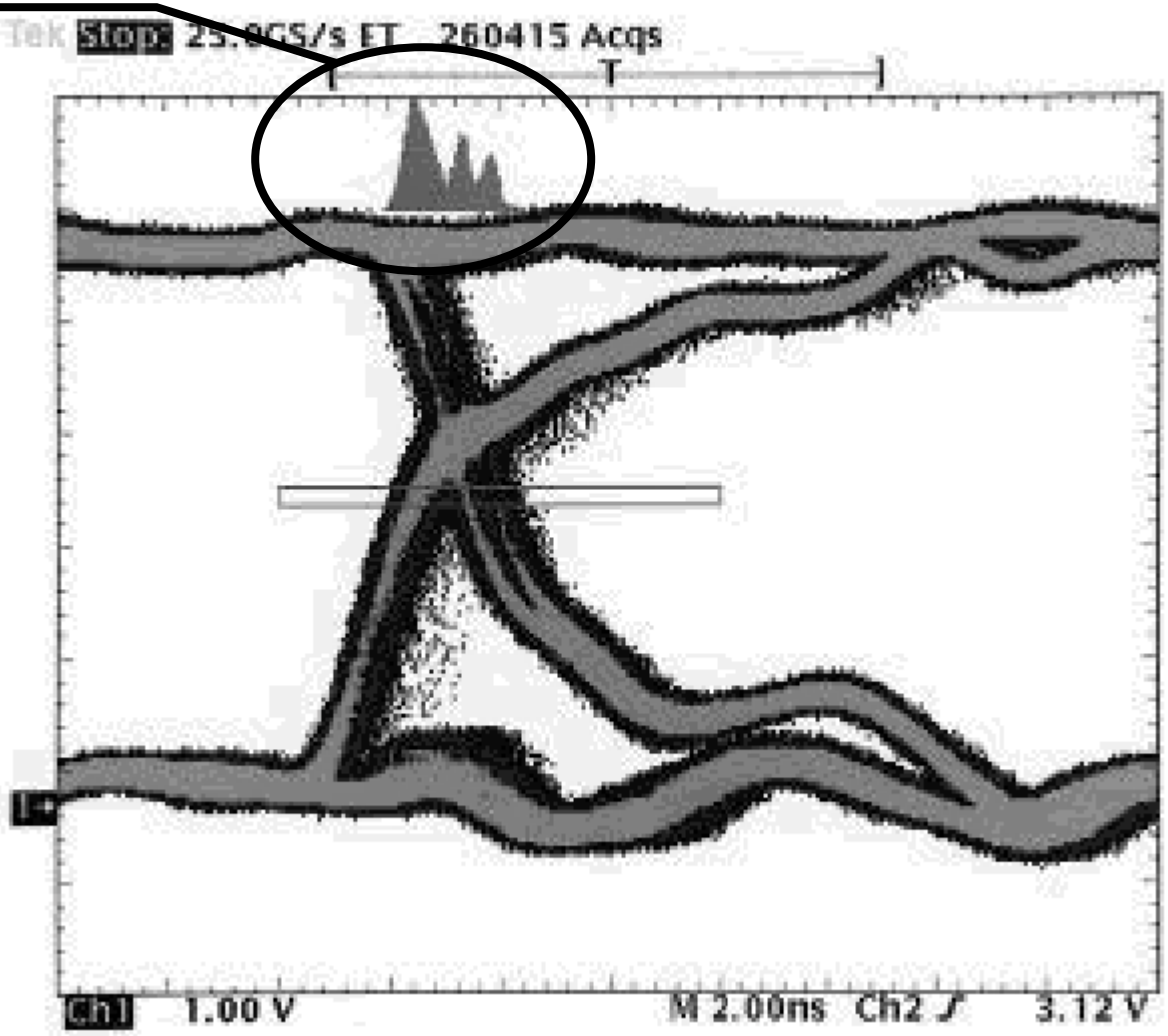
Jitter Analysis of Data Communication Devices

Overview of Section 2

- Review of Jitter components
- Why specify Jitter?
- Jitter in networks
- Introduction Jitter Specifications
- Jitter Output Testing
  - Methodologies for accurate compliance testing (FC-PY)
- Jitter Transfer Testing
- Jitter Tolerance Testing

Traditional View of Jitter on Data

Total Measurement Histogram



FC - Total Jitter Calculation

(Using Golden PLL and Eye-Histogram™)

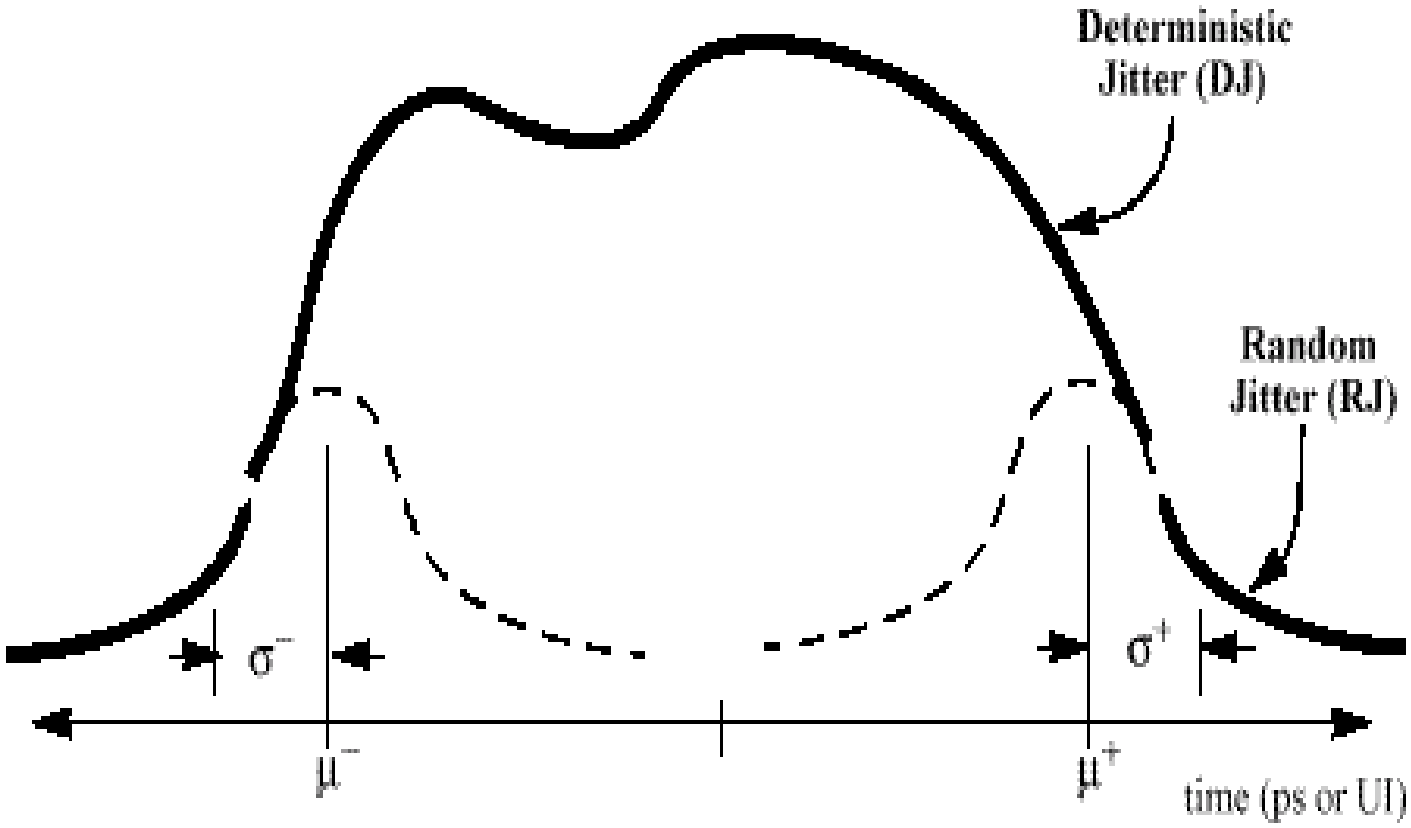
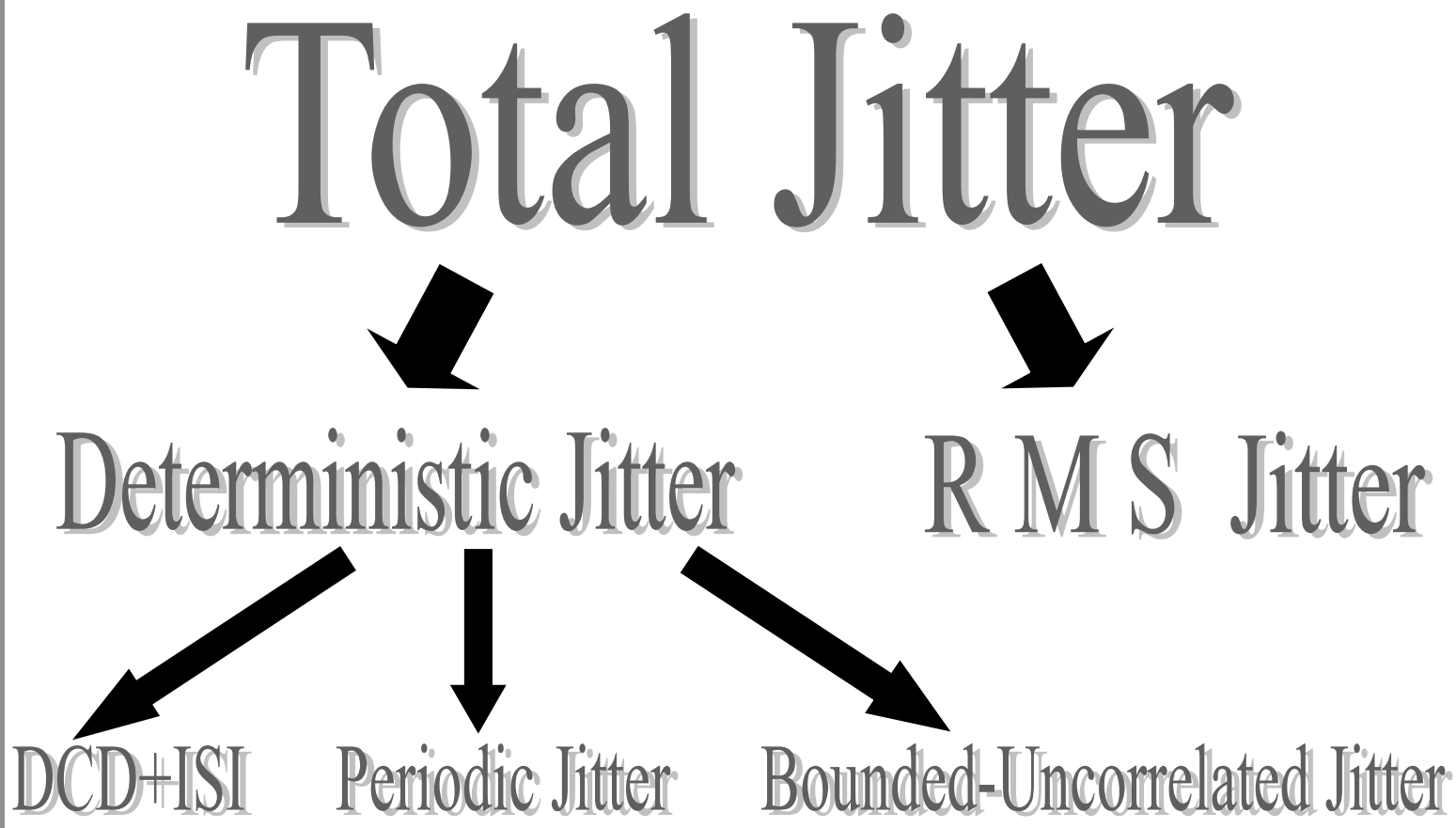


Figure D.1 – Time Domain Total Jitter Calculation

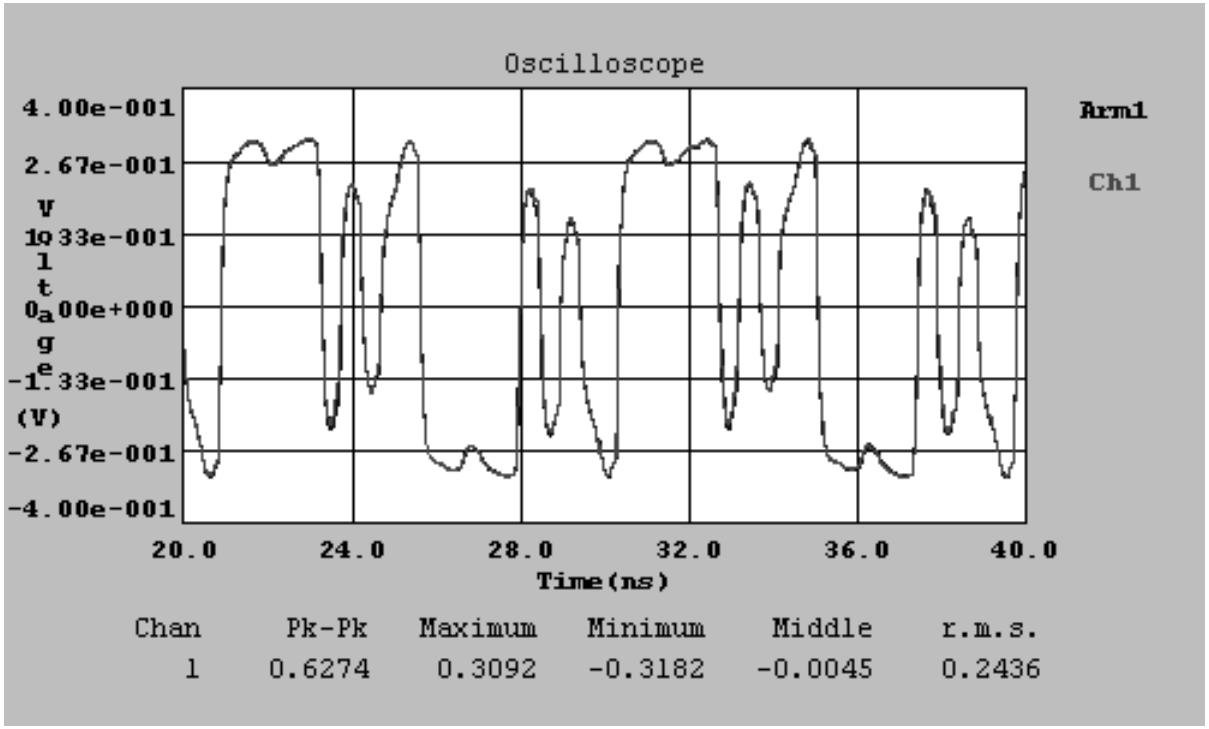
Jitter Terminology Review



Jitter Terminology Review

- Deterministic Jitter (DJ)
  - DJ is bounded and effects short term stability
  - Composed of Duty Cycle Distortion (DCD), Inter-Symbol Interference (ISI), Periodic Jitter (PJ) and Bounded Uncorrelated Jitter (BUJ)
  - DCD & ISI
    - Can quantify the quality of the interface and the Input and Output impedance matching
    - Typically caused by bandwidth limited media or driver in transmitter.
  - PJ
    - Can quantify cross talk effects from EMI sources and adjacent or nearby signal paths and quality of clock source.
    - Signals sharing media, such as in DWDM configurations or in network switches, can sometimes be susceptible to cross talk contamination. SONET switches supporting multiple standards exhibit some level of PJ at relevant frequencies.
- Random Jitter (RJ)
  - RJ is unbounded and is best described by a Gaussian distribution.
  - RJ is indicative of process impurities and Gaussian noise sources in the path of transmission.

Bandwidth and DDJ



- Data Dependant Jitter (DDJ)
  - Duty Cycle Distortion and Inter Symbol Interference are examples of data dependant Jitter
  - The picture above is an example of bandwidth effect on a serial data stream
    - Notice that the voltage amplitude is a function of the duration of the state

Extracting Bit Error Rate (BER) from Jitter

Jitter to BER…It is all in the Math!

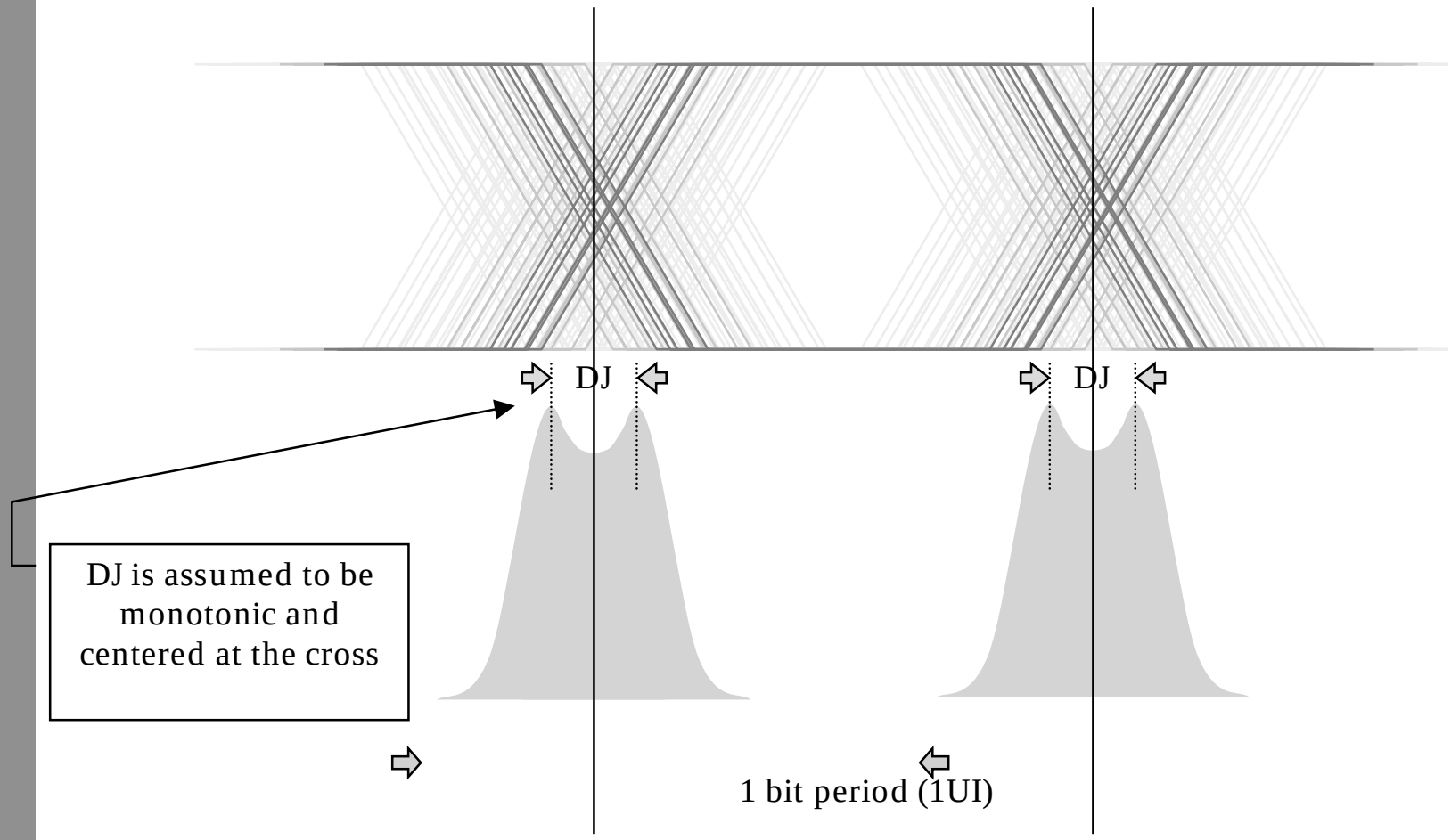
- Total Jitter :
  - *"The total jitter is the sum of the peak to peak values of deterministic jitter and random jitter."* Fibre Channel MJS-10, page 8.
  - *"Jitter is the mis-positioning of the significant edges in a sequence of data bits from their ideal positions. Sufficiently gross mis-positioning results in data errors."* Fibre Channel MJS-10 page 7.
  - Total Jitter is the convolved sum of Deterministic Jitter and Random Jitter. Accurate convolution results in the accurate estimation of Total Jitter for a given Error Density.
    - Fibre Channel specifications are based on a 14σ reliability level.

$$TJ = DJ * 14 \times RJ$$

(Where "*" indicates "convolved with")

  - As a simplification, a "double delta" model of total jitter can be used
    - *Please note, a double delta model, oversimplifies the deterministic jitter total quantification and can lead to a grossly underestimation of deterministic jitter.*

Basics of the "Double Delta" Model



This simplification allows the engineer to visualize the summation of DJ and RJ as follows:

$$TJ = DJ + n \times RJ$$

Where "n" is equal to the σ level of reliability (n=14 for 14σ reliability)

Real DJ Model

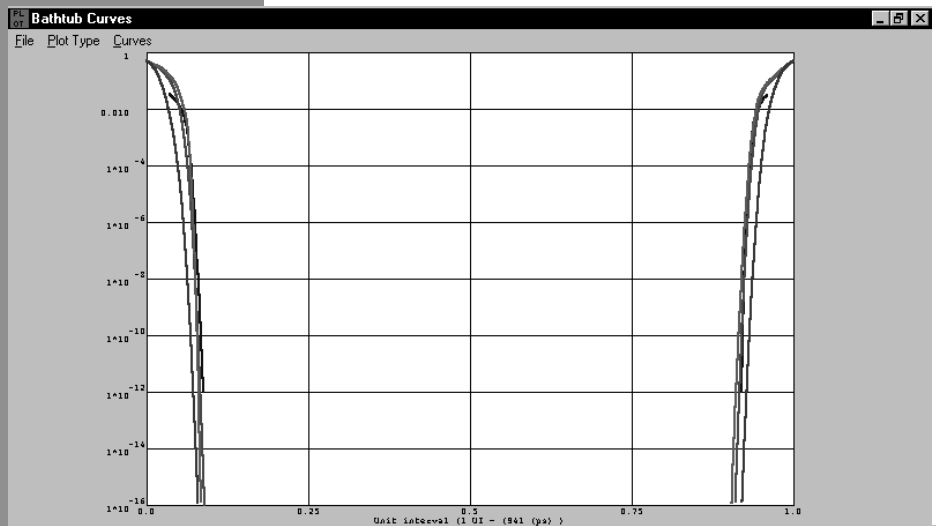
- "Double Delta" is too simple.
  - Typical DJ effect is a combination of data dependant jitter (DDJ) components and periodic jitter (PJ) components.
  - Extrema components of Random Jitter do not always add linearly to the extrema of periodic. There is a probabilistic component to the summation. Therefore

Convolution is best approximation of RJ – DJ interaction

- Convolution Mathematics
  - Unlike linear summation, convolution accounts for phase relationship of discrete jitter components. J
    - *Note: All jitter components can be approximated by transfer functions in the time domain. The following equation describes how to convolve two time domain transfer functions*

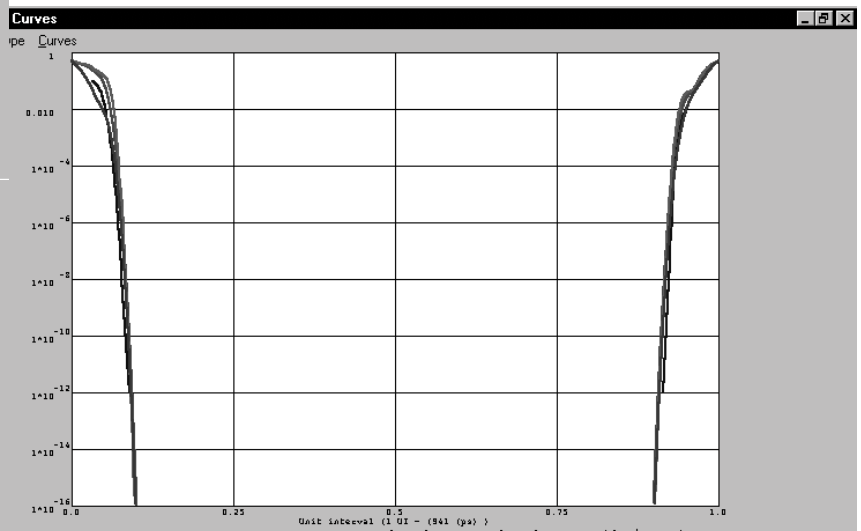
$$\mathbf{f(t) * g(t) = \int_{-\infty}^{+\infty} f(\tau)g(\tau - t)d\tau}$$

Correlating to Reality



	DCD+DDJ	PJpk-pk	DJpk-pk	RJ(1sigma)	TJ
DTS Data COM	94.668	4.273	98.942	4.569	156.865
DTS Eye Histogram					
Data - Clock			106.322	4.029	159.226
Clock			5.893	3.449	47.678
DTS No Clock/No Marker			72.042	5.193	136.059
HP BERT					157.385

- Correlation study to the left shows a 500fS difference for TJ between BERT and Eye Histogram for BER of 10^{-12}
  - This is less than a .05% error
  - Eye Histogram uses same Clock to Data relationship as BERT.
  - This Correlation Study proves the validity of the convolution method proposed in the MJS document.

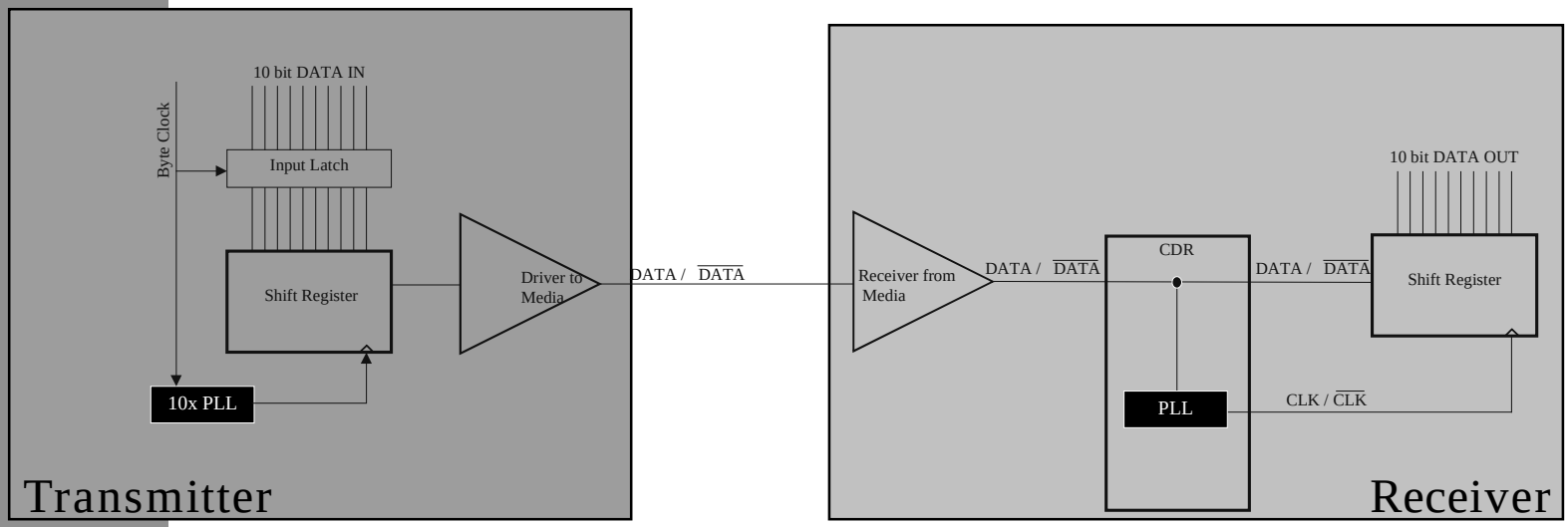


	DCD+DDJ	PJpk-pk	DJpk-pk	RJ(1sigma)	TJ
DTS Data COM	103.753	4.175	107.928	5.344	175.898
DTS Eye Histogram					
Data - Clock			109	4.762	172.041
Clock			5.726	3.382	46.444
DTS No Clock/No Marker			105.731	5.376	172.078
HP BERT					163.871

- Correlation study to the right is for PRBS 2^7-1 while the above study is for a MRPAT
  - See www.t11.org or www.wavecrest.com for further details on correlation between convolution of Jitter components and BERT

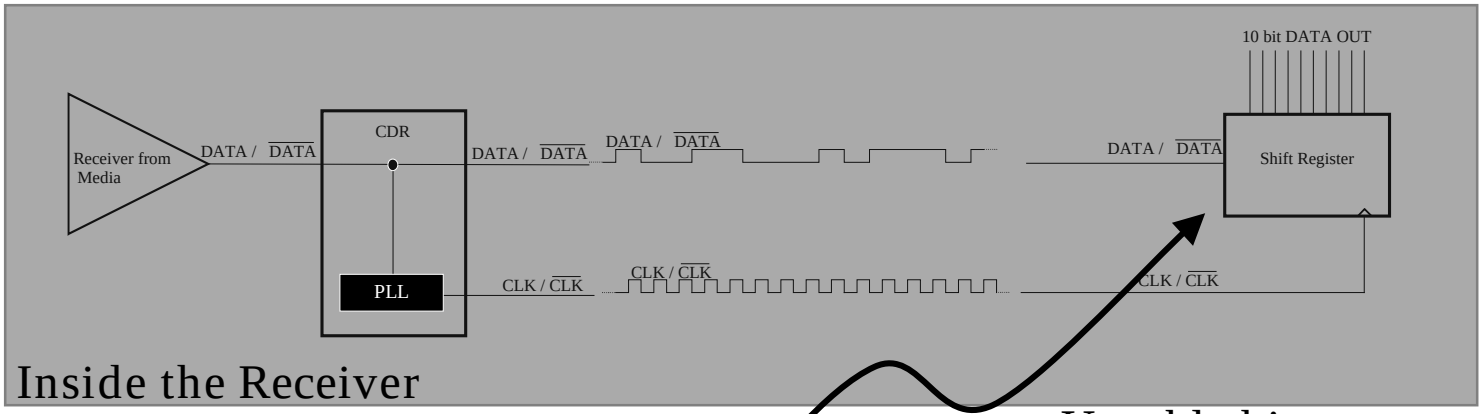
The Making of a Jitter Specification

Typical Receiver/Transceiver Pair

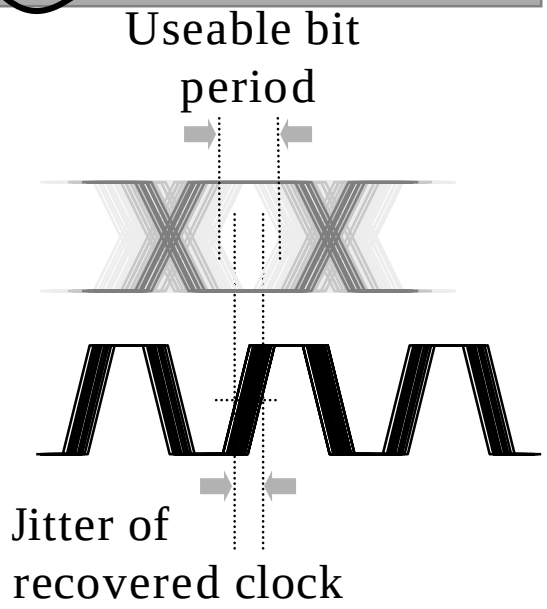


- For accurate data transmission
  - Receiver must accurately identify the data bits in the sequence they were sent.
  - Any jitter or clock timing error originating in the receiver must be accounted for in the useable bit period at the shift register.
    - The recovered clock edge in the receiver must arrive at the shift register within the useable bit period. Otherwise, the data from the wrong bit period will be captured.
  - For interoperability to be insured, proper limits leading up to the receiver must be established and adhered to.

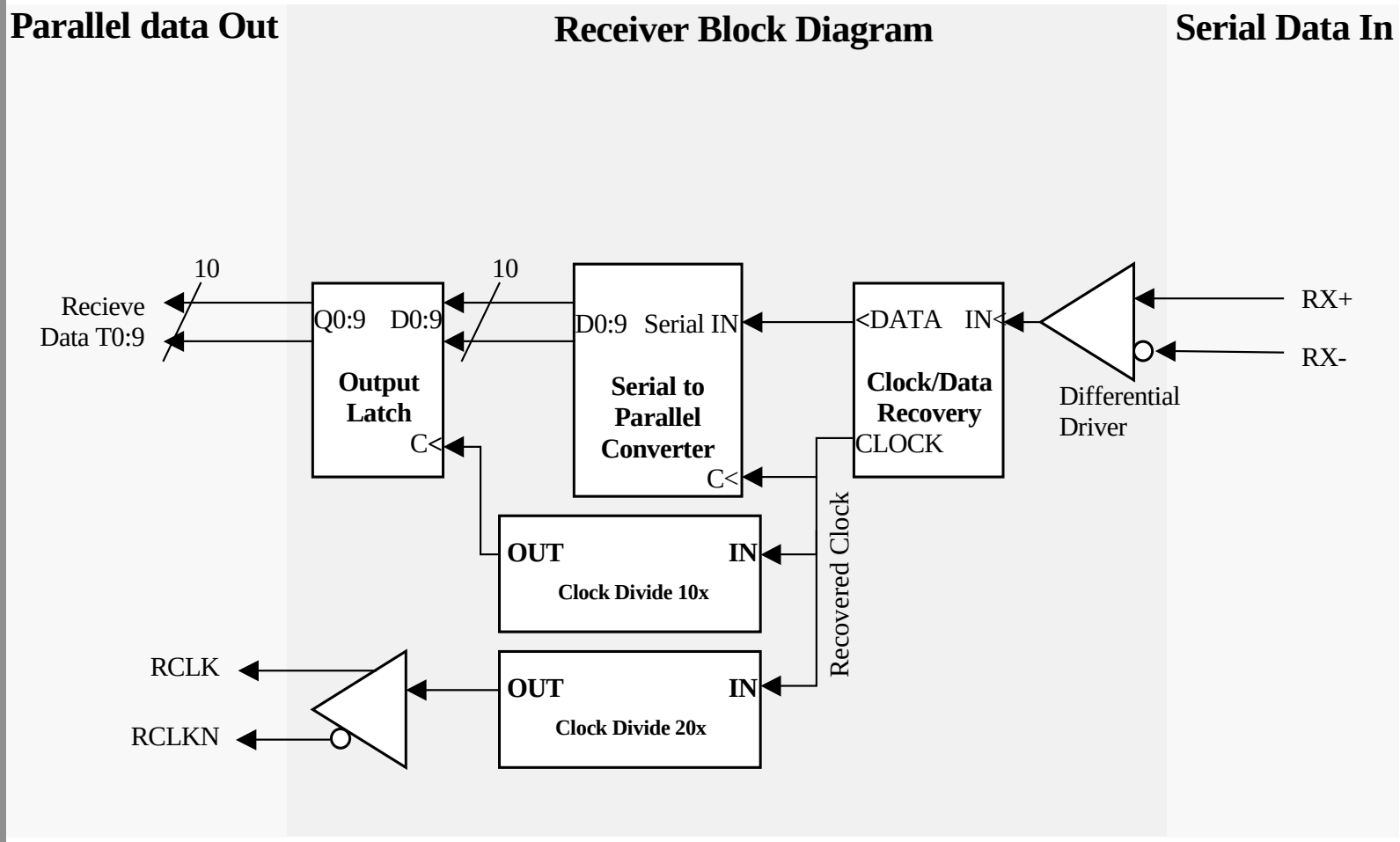
Receiver design dictates jitter component (RJ,PJ,DJ,TJ) tolerance levels



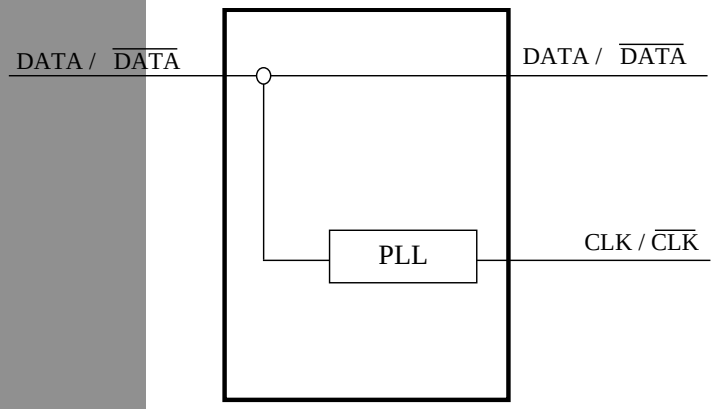
- Effect of jitter on data stream at the SERDES interface results in a reduction in the useable bit period.
- Jitter of recovered clock must fall within the remaining useable bit period.
- Useable bit period is equal to the eye opening at a desired bit error rate.



Typical Receiver Block Diagram

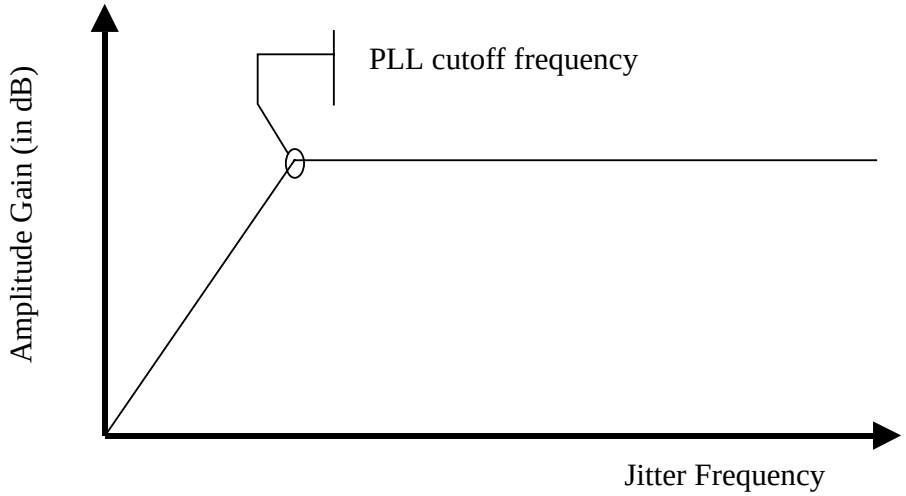


Typical Clock Data Recovery Device

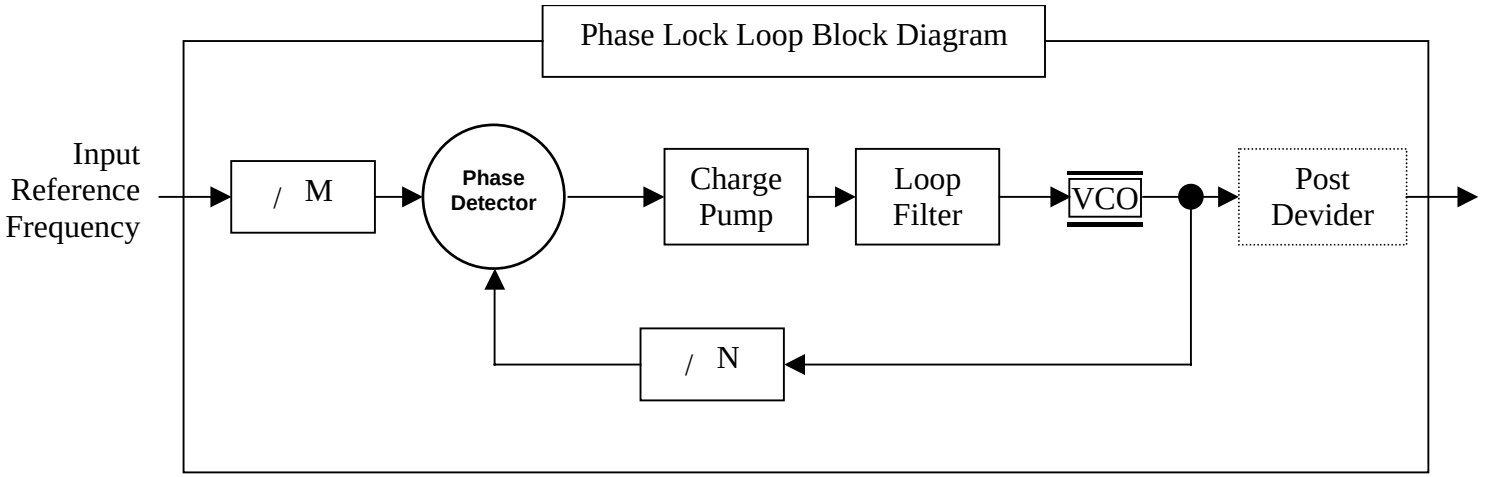


- Typical CDR composed of data pass through and clock extraction circuit (typically a PLL)
- Clock is used to trigger de-serializer
- Data is sampled by de-serializer at prescribed delay from the reference edge of clock.

- PLL in CDR has a characteristic frequency response. Frequencies below this cutoff frequency are tracked by the PLL and passed through to the de-serializer.
- Frequencies above the cutoff frequency are masked out and are not passed to the de-serializer

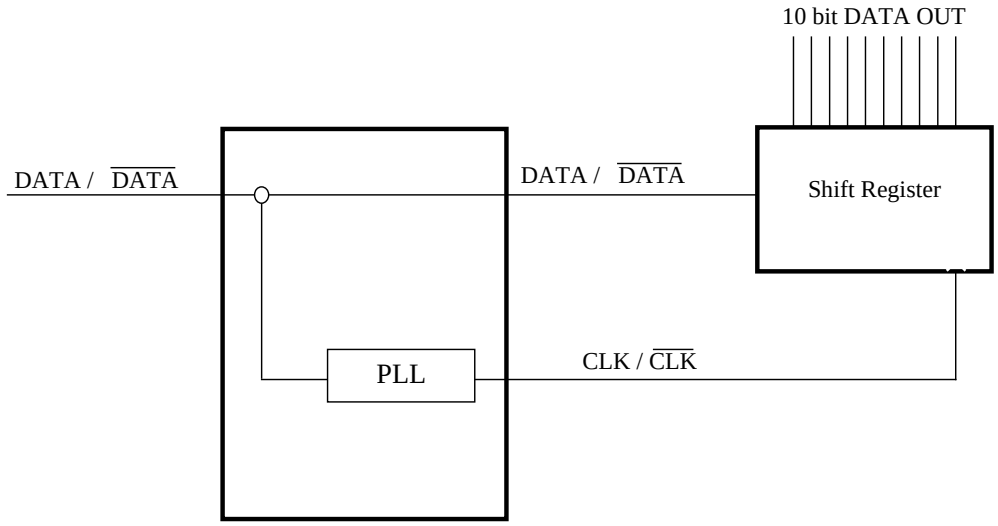


Fundamentals of a PLL



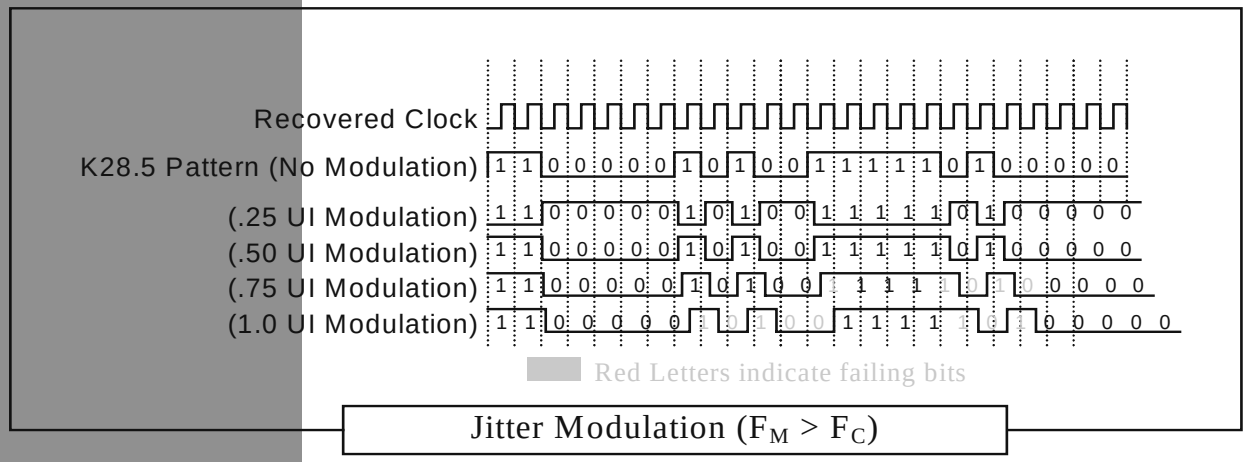
- **Output Frequency = F_{REF}*P/N**
  - If a Post divider is used, the output frequency is scaled accordingly
- **The Charge Pump and Loop Filter are responsible for establishing the voltage on the VCO thereby establishing the output frequency of the VCO.**
  - VCO voltage is established based on the phase and frequency relationship of the feedback loop and the input reference frequency.
- **The loop response of the PLL is a function of the loop response through the feedback divider (N).**
  - Loop response of the PLL defines the low frequency cutoff detection of the receiver in which it is used. Low frequency cutoff in a receiver is that modulation frequency below which modulation will not effect eye opening.

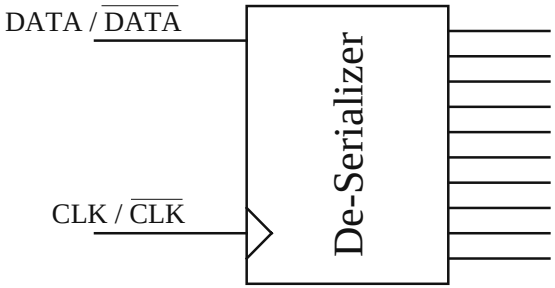
How Jitter Affects Receiver



- All jitter on the data stream is fed into shift register (de-serializer)
- High frequency jitter (Jitter Modulation above F_c) is filtered off of clock signal. (PLL is not tracking it.)
- Recovered clock is used to latch data in Shift Register.
- Jitter between recovered clock and data can cause the wrong data to be latched in the shift register.
- Bandwidth limiting effects resulting in ISI Jitter on data will not be observed on the recovered clock.

Effect of PJ on De-Serializer





- For Periodic Jitter Frequencies above the PLL cutoff frequency, De-Serializer may not capture the accurate data.
  - Data will still have the modulation component adjusting the time at which the transition occurs.
  - Clock signal will have filtered out the modulation since it cannot track the modulation frequencies above it's cutoff frequency.
- THEREFORE: Jitter Specifications are defined in terms of amplitude and frequency.

Fundamentals of Jitter Specification

- Jitter Specifications start with defining the performance of the Receiver. Useable bit period at the receiver is the fundamental metric for performance.
- TJ Specification
  - The TJ budget dictates the amount of useable bit period available to the receiver.
    - Useable Bit Period (Eye Opening) = Bit Period – TJ@BER
- PJ Specification
  - Magnitude of periodic Jitter is dependant on frequency of modulation.
    - Cutoff frequency of PLL in receiver dictates the low frequency modulation tolerance of the receiver.
    - Maximum Amplitude of PJ component above CDR-PLL cutoff is a function of total DJ tolerance of the given interface. Various governing bodies establish limits for total DJ over a given frequency band.
- RJ Specification
  - Magnitude of RJ is based on the Total Jitter at a given Error Rate.
    - TJ is essentially the inverse of the useable eye opening at a given error rate. Since TJ is composed of both RJ and DJ, governing boards must decide adequate limits for at least TJ.

Examples of Jitter Specification

- Fibre Channel –
  - We will use Fibre Channel MJS specification as an example of data signal jitter specification. Other protocols use different methodologies for specifying the same thing. Namely, useable bit period at the deserializer of the receiver.
    - SONET, for example, uses a combination of spectral peaks and RMS of jitter within various frequency bands. This technique is very time consuming and requires quite specific test setups to properly measure jitter compliance. Each setup is specific for a given frequency band and for specific bit rates.
      - Traditional SONET test methods require the analysis of the recovered clock. This can be very difficult to do without a "golden PLL" for accurate clock regeneration.
      - SONET ATM and packet switched VoIP are currently competing for protocol dominance in the >10Gbps arena. Which ever protocol wins will probably establish the telecommunication standards for many years to come.
      - SONET standards and methodologies are addressed in a separate telecom jitter training jitter module.
  - Fibre Channel compliance for jitter is established through maintaining specific DJ and TJ limits at various points along the communication path known as "Compliance Points."
  - Note: much of the MJS rev 10 specification is focused on the 1.0625Gbps speed. See the relevant ANSI specification for other protocol limits.

Compliance Points

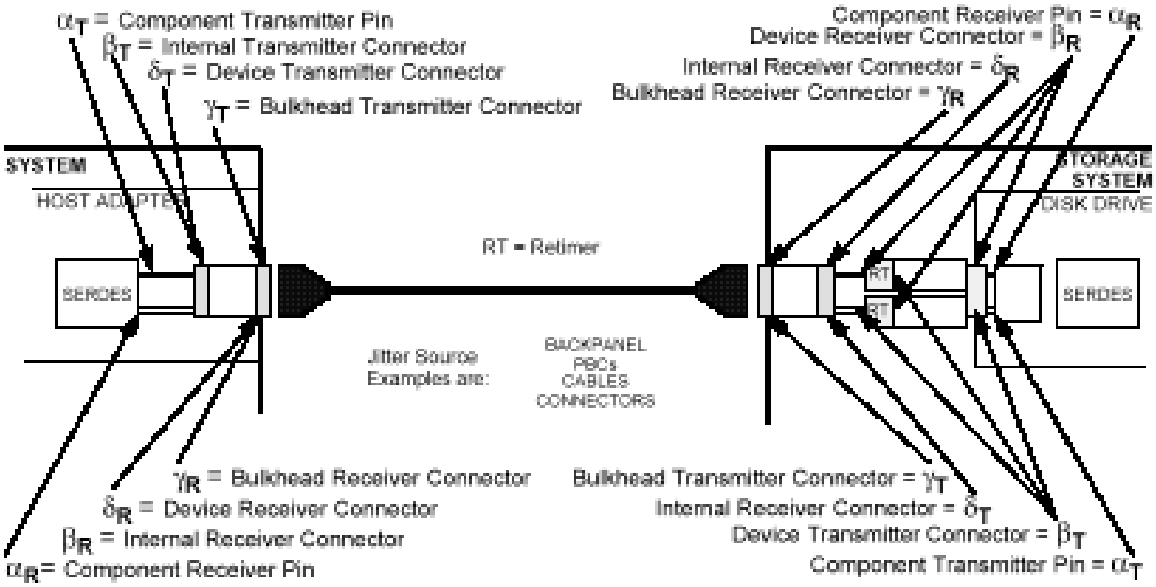


Table 6 – 1,0625 GBaud jitter output allocation (Passband of 637 kHz to greater than 5 MHz)

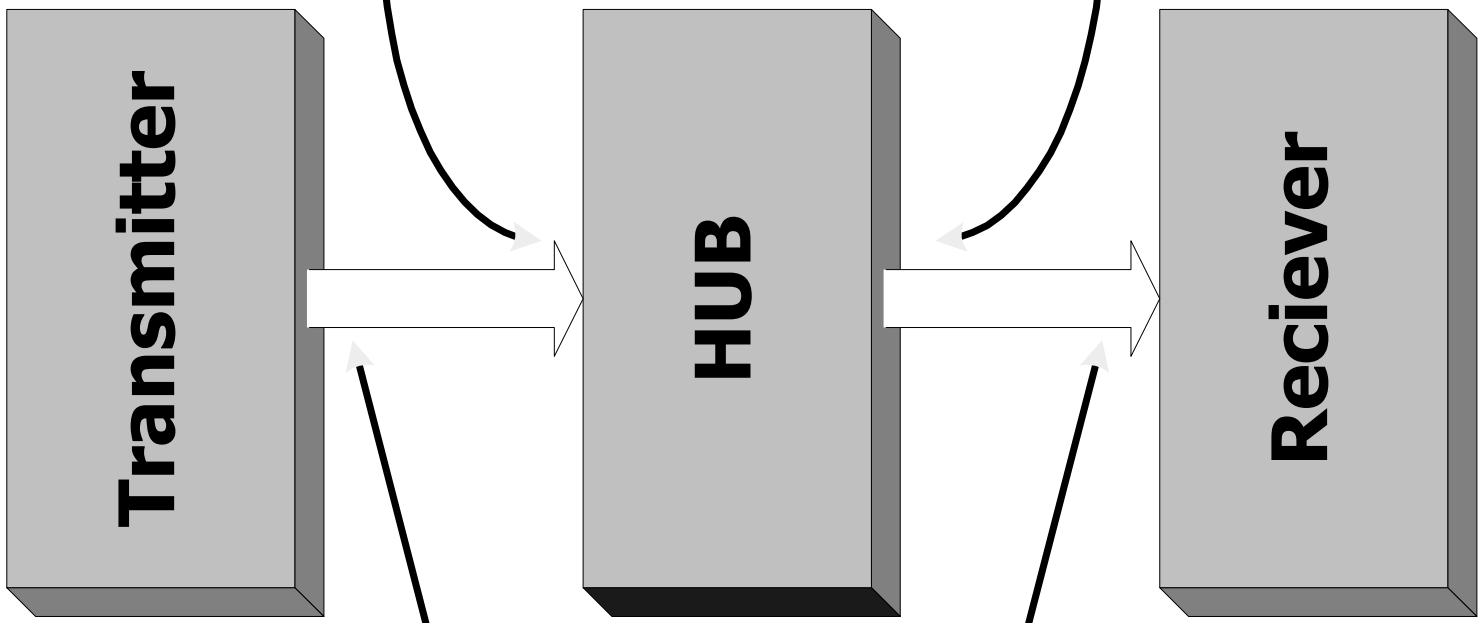
Variant	Jitter (Unit Interval - UI)								
	Component	α_T	β_T	δ_T	γ_T	γ_R	δ_R	β_R	α_R
100-SM-xx-x (single mode)	DJ	0,10	0,11	0,12	0,21	0,23	0,36	0,37	0,38
	Total	0,21	0,23	0,25	0,43	0,47	0,61	0,63	0,65
100-Mx-xx-x (multi-mode)	DJ	0,10	0,11	0,12	0,21	0,24	0,36	0,37	0,38
	Total	0,21	0,23	0,25	0,43	0,47	0,61	0,63	0,65
100-xx-EL-x (copper)	DJ	0,10	0,11	0,12	0,13	0,35	0,36	0,37	0,38
	Total	0,21	0,23	0,25	0,27	0,54	0,56	0,58	0,60

Fundamentals of Jitter Testing

Jitter Output (Generation),
Jitter Transfer and Jitter Tolerance

Introduction to Jitter

Jitter Transfer is measured as the net gain between these two points.

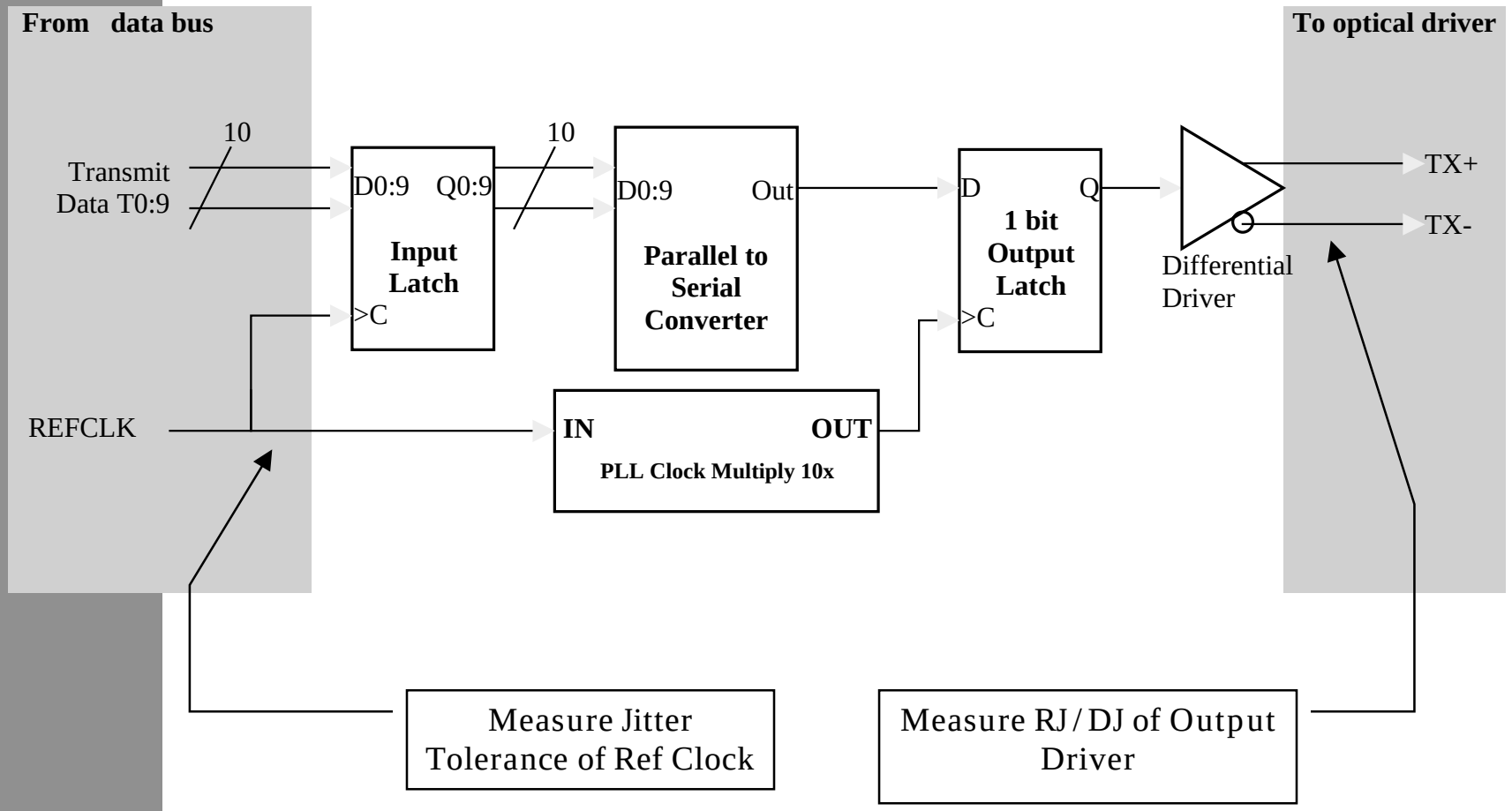


Jitter Output is measured at this point.

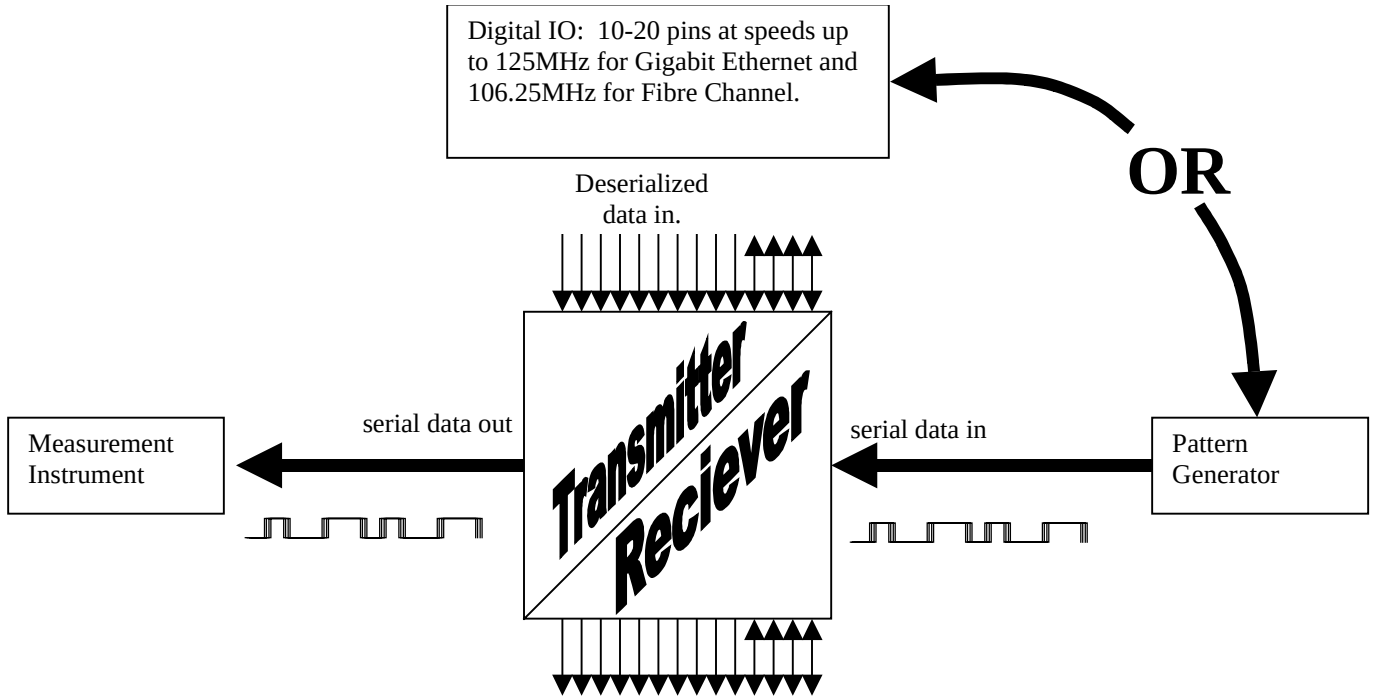
Jitter Tolerance is measured at this point

Jitter Testing of Transmitter

Typical Transmitter Block Diagram

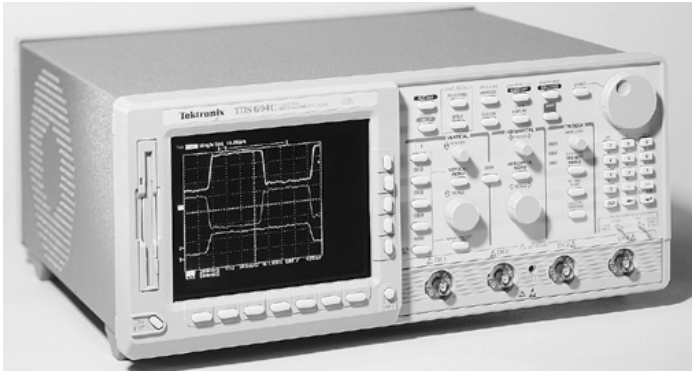


How to Connect

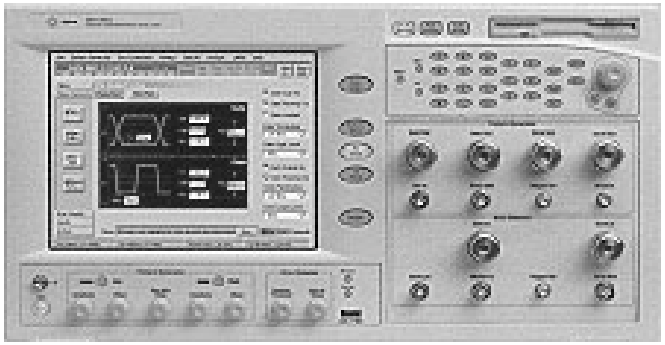


- Set control bits to allow data transfer from either Receiver in (bypass mode) or from Transmitter buffers.
  - Use looping pattern
  - Provide pattern marker (for Wavecrest)
  - Provide golden PLL for compliant CDR (for BERT or O'scope)

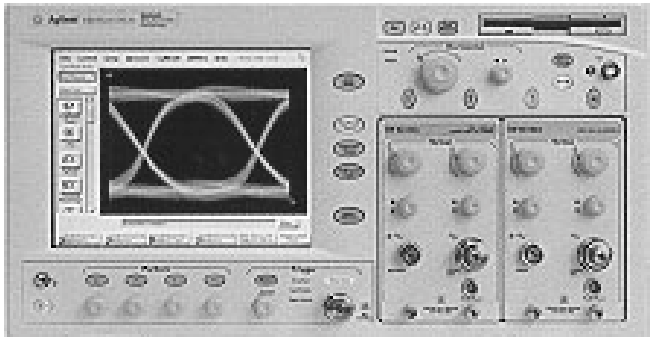
Possible Solutions



Cannot use a Digitizing Oscilloscope

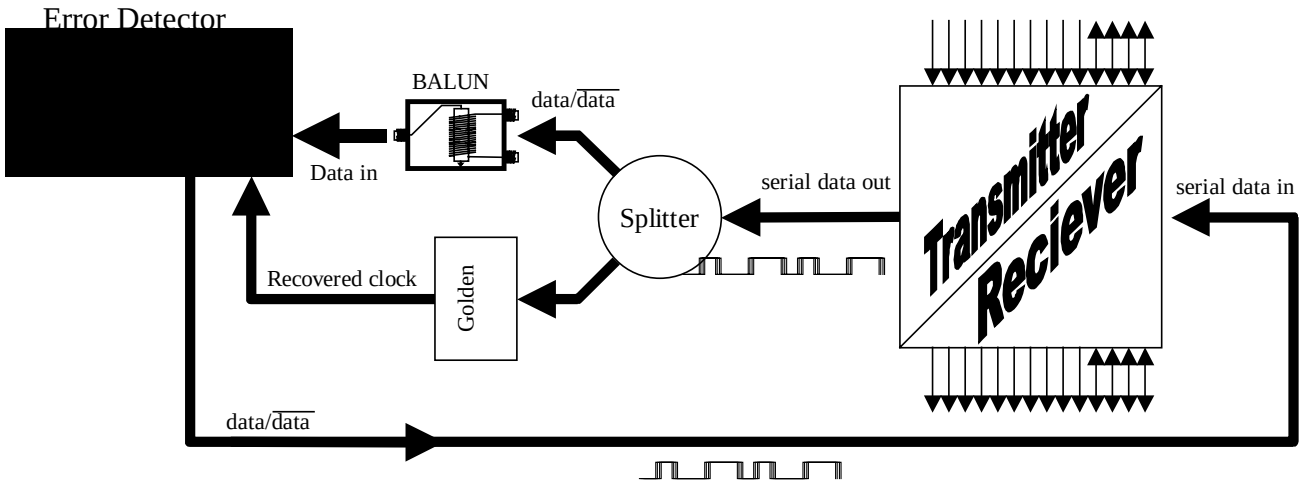


(with FC compliant CDR(Golden PLL) for triggering)



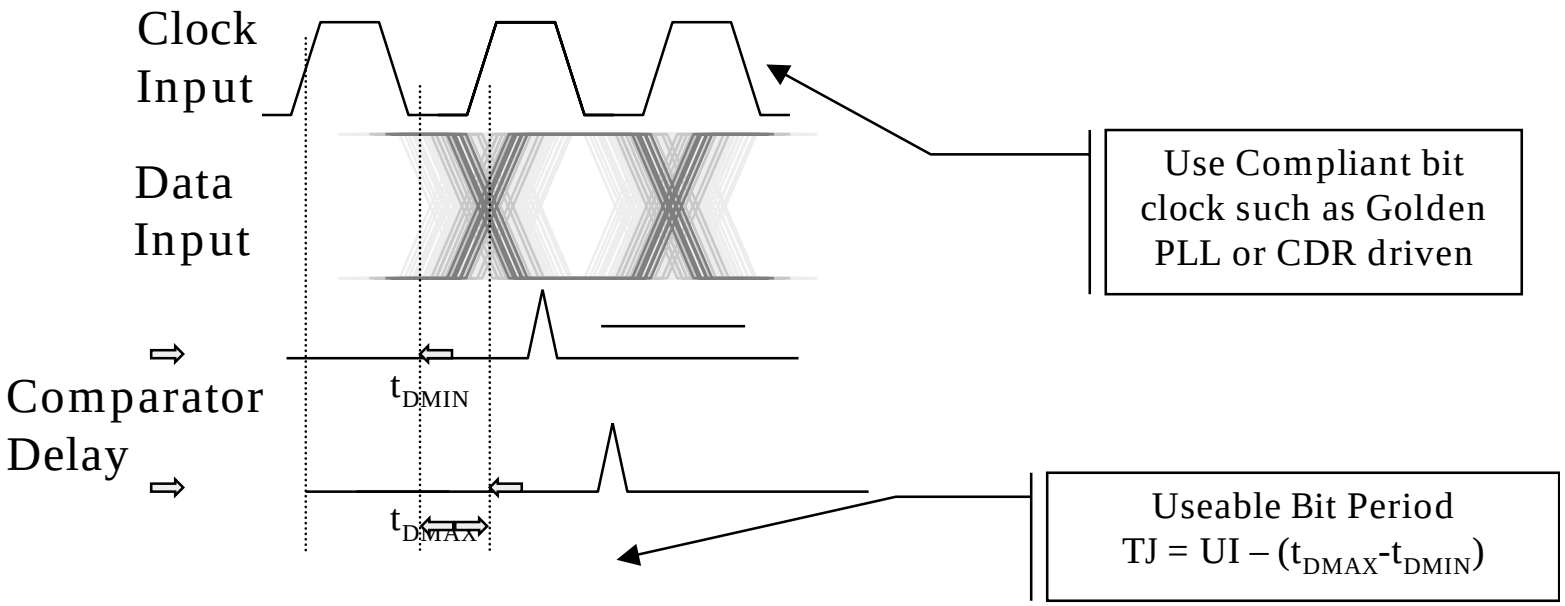
(with FC compliant CDR(Golden PLL) for triggering)

Using a BERT



- Bit Error Rate Tester (BERT)
  - Requires Golden PLL (compliant CDR with specified frequency response characteristic)
    - For Fibre Channel, this would be a PLL with a loop response of 637kHz
  - Using BERT's clock for data triggering could cause false readings
    - Clock is synchronous with data
    - May mask periodic components originated in test equipment or may not mask PJ components which are acceptable (below F_C)

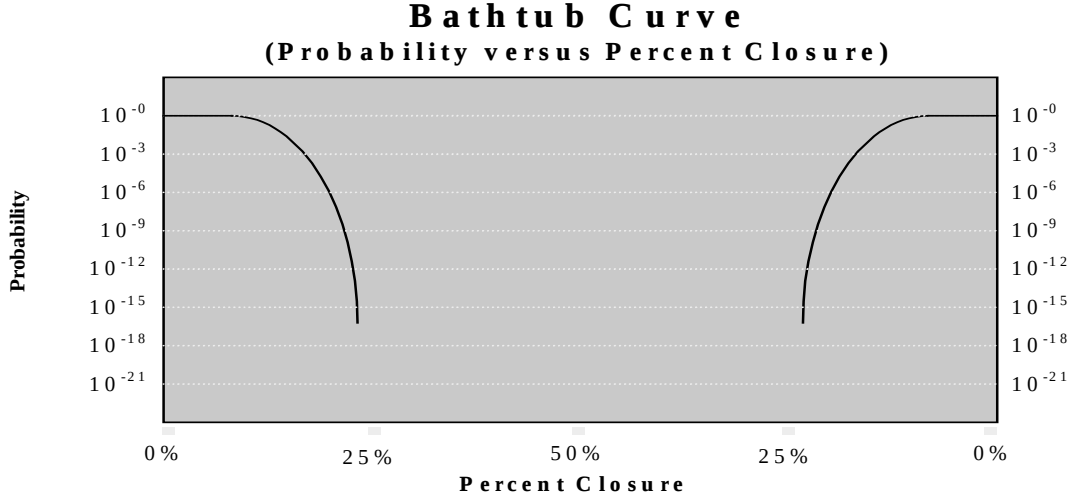
Using the BERT for Total Jitter Measurement



- Bit Error Rate Test (BERT) Systems
  - Adjust Comparator delay to find t_{DMAX} and t_{DMIN} for bit error rate (BER) in question (14σ for Fibre Channel Compliance)
  - Subtract (t_{DMAX}-t_{DMIN}) from Unit Interval (UI) to get Total Jitter (TJ) at given BER
  - Be sure to execute through entire reliability level desired (for 14 σ reliability, test at least 10^{12} cycles of data)
    - for Fibre channel, each pass = 941.7 seconds (@1Gbps)
    - may take several passes to find pass / fail boundary

Result = Total Jitter

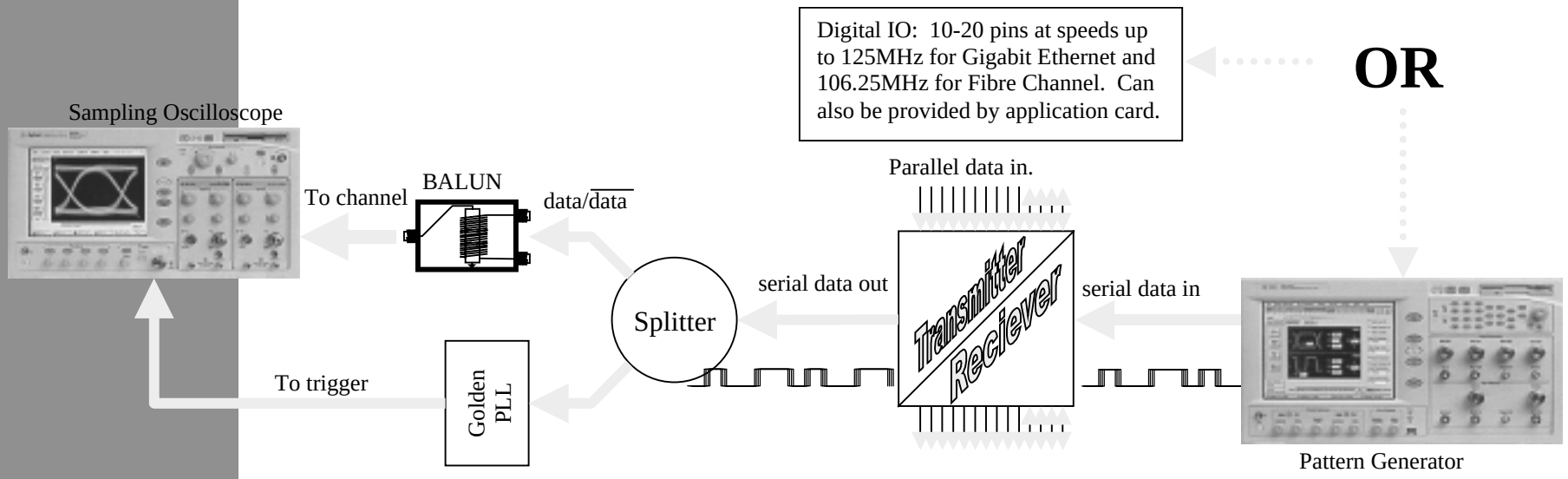
Developing Bathtub curve from BERT data



- Bathtub curves show TJ versus Error Probability
  - Can be generated from BERT data based on TJ values and the associated BER with the TJ level
  - BERT should not be used for high BER areas of Bathtub curve
    - RJ/DJ de-convolution is impossible without time domain relationship information of DJ components and RJ component
    - Use BERT based bathtub curve only for BER above 10^{-6}
  - If no low occurring DJ is present, TJ can be extrapolated from BERT bathtub curve
    - Obtain TJ data for BERs of 10^{-6}, 10^{-7}, 10^{-8}, and 10^{-9}. Then extrapolate curve to 10^{-6} for TJ at 14σ

See www.wavecrest.com for a correlation study of using this method.

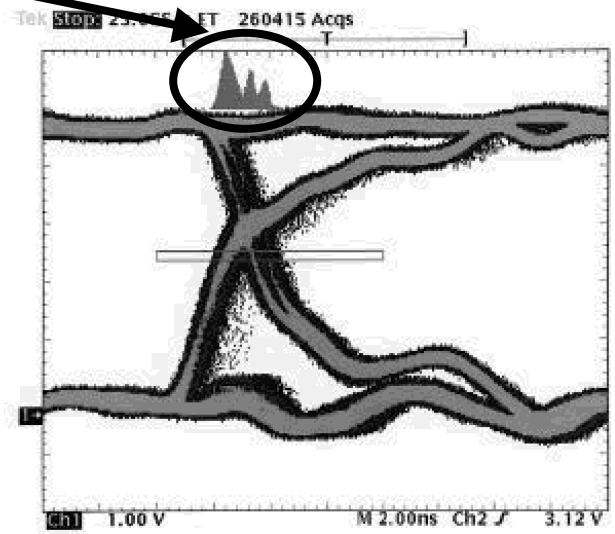
Using Sampling Oscilloscope

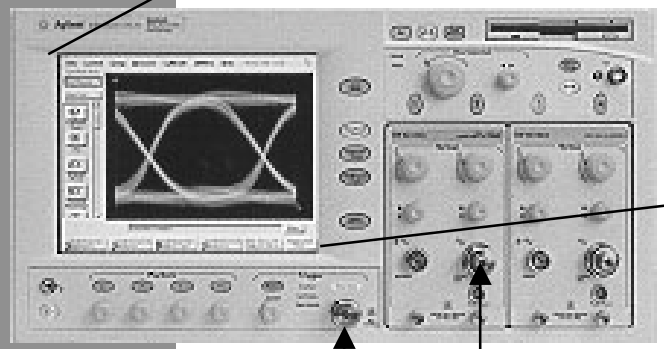


- Sampling Oscilloscope measures clock to data jitter
  - Since the measurement is triggered against the clock signal, the jitter measurement is actually the clock to data jitter. This may or may not be representative of the actual jitter on the data stream.
    - In order to best approximate the result, be sure use a golden PLL.
  - Jitter Result will be Total Jitter peak to peak. No Jitter Separation available for oscilloscopes.
  - Number of hits is inversely proportional to desired BER. Therefore, be sure to take enough data to display 10^{12} hits at the transition point. (On many scopes, this will take several hours, so, only do this during after hours!)

Oscilloscope's View of Jitter on Data

Total Measurement Histogram



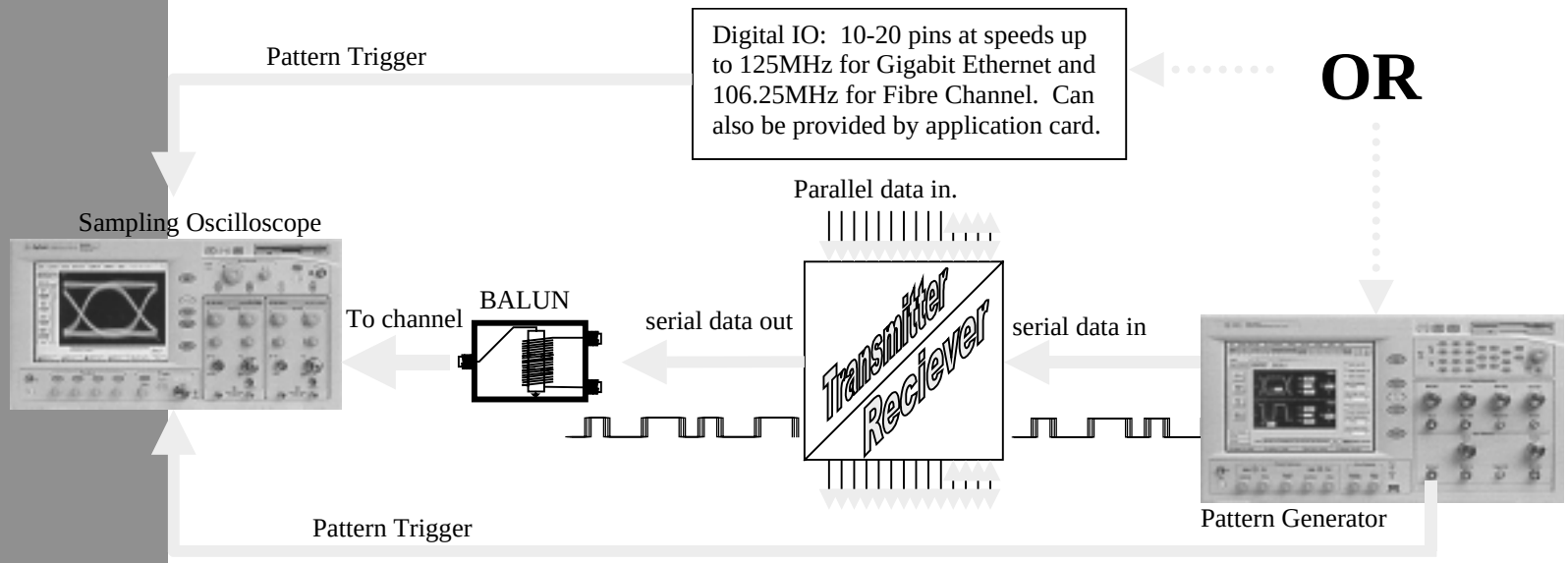


Single Ended Data Stream

Recovered Clock

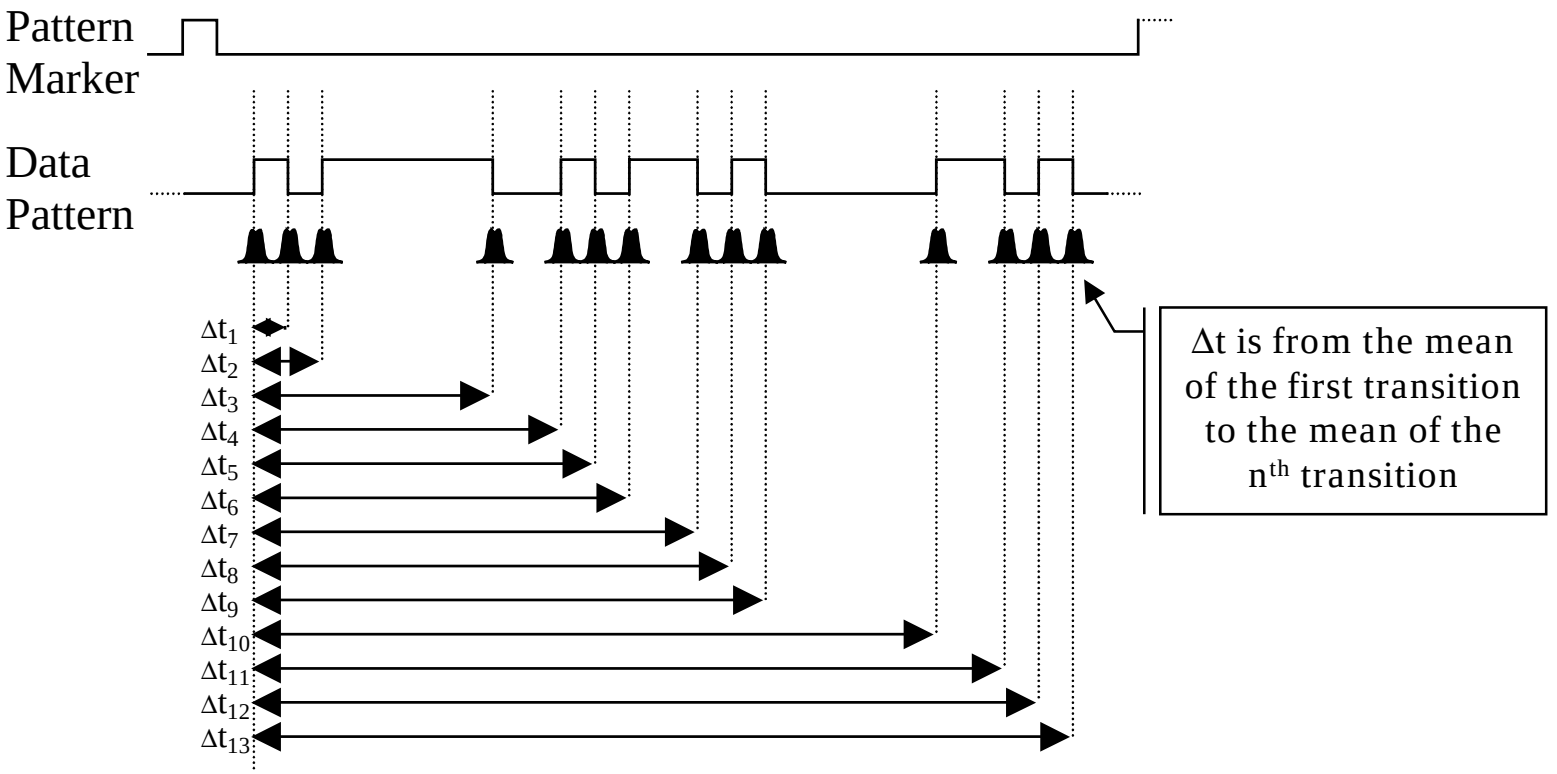
- **This Histogram shows the relationship of the recovered clock to the data stream. This is not the jitter on the data.**
- **Keep in mind that the scope delay may mask high frequency components.**

Using the O'scope for DDJ



- Data Dependant Jitter
  - The Sampling Oscilloscope is ideal for Data Dependant Jitter testing on data patterns less than 1024 bits long.
    - Time base drift will adversely affect accuracy on time measurements above 1µs. Oscilloscope time base stability varies from scope to scope. Check with your scope vendor for details.
  - Trigger Oscilloscope on Pattern Marker instead of bit clock for clear picture of each transition.
  - Take enough points such that at least 500 hits occur at each transition point

Data Dependant Jitter with Oscilloscope

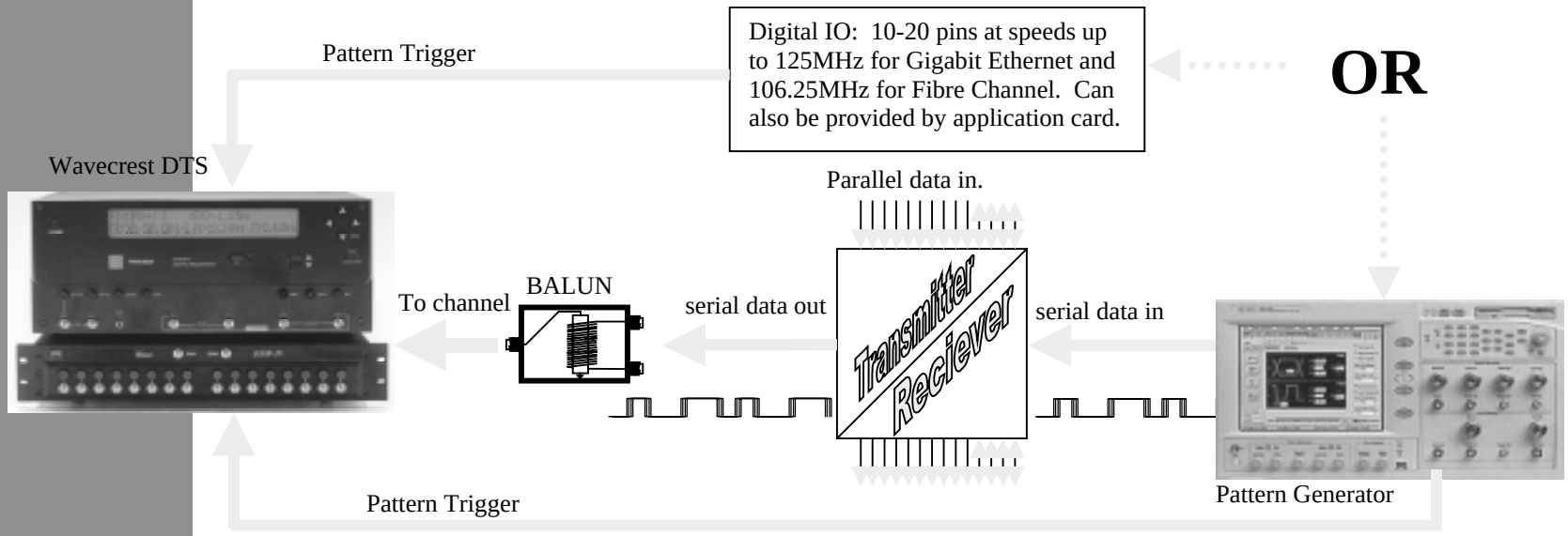


- Data Dependant Jitter (DDJ) is worst case off set of mean from ideal as follows:

  $DDJ_n = \Delta t_n -$ m x UI (where m = number of bit periods included)

  DDJ = Maximum DDJ_n – Minimum DDJ_n

Using Wavecrest DTS to Analyze Jitter



- Separation of Jitter Components
  - RJ, DCD+ISI,PJ and BUJ
- Quick Correlation
  - Laboratory, Production and Customer Application Card
  - Share Setup files and data files to compare various setups
  - Minimize operator setup error
- Characterize PLL Bandwidth and Loop-Feedback Response Time

Wavecrest's VISI Toolset

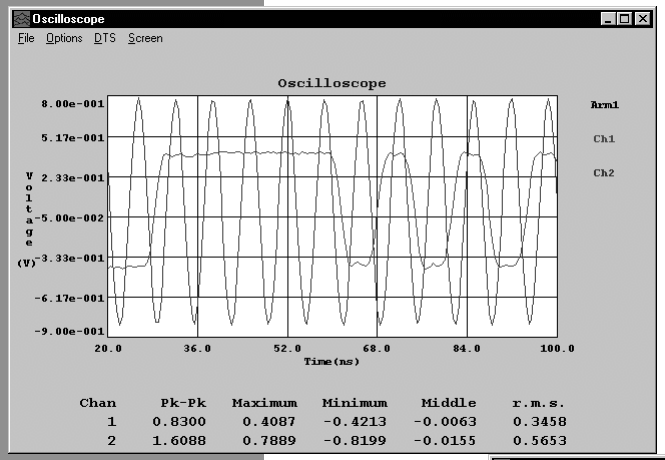
(And now a word from our sponsor…)

Get the VISI advantage

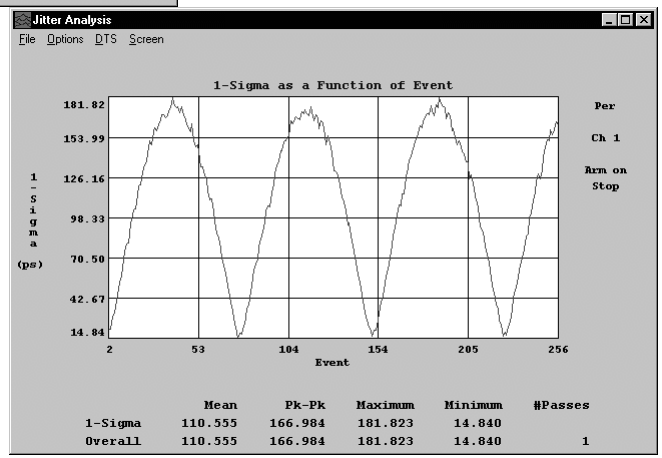
Clock Analysis Tools

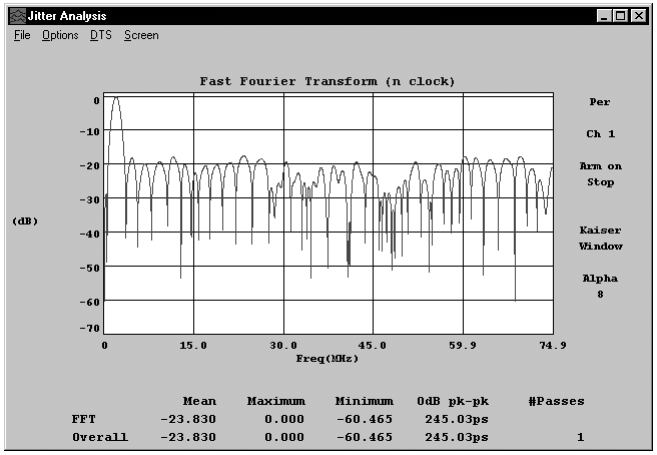
- Predict Short-Cycle events based on proven Gaussian mathematics
  - *"How often is the clock period too short?"*
    - Use VISI 5.0 and find out how short is short.
- Predict Jitter specification violation
  - TailFit™ can estimate the probability of experiencing both long cycle and short cycle errors independently for true reliability modeling.

Clock Jitter Analysis



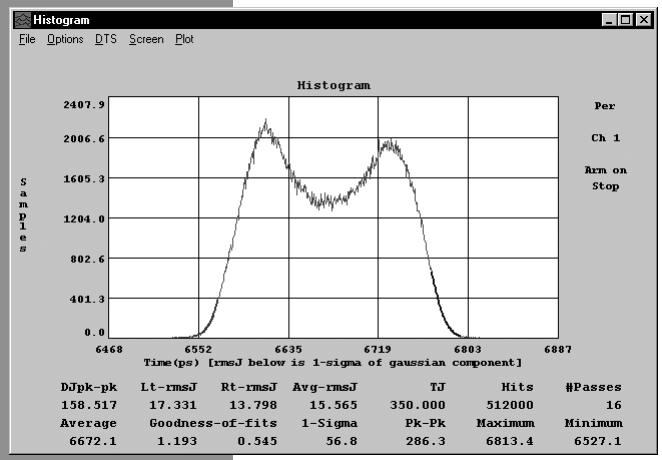
From Oscilloscope view to modulation domain plots for easy Jitter Analysis.





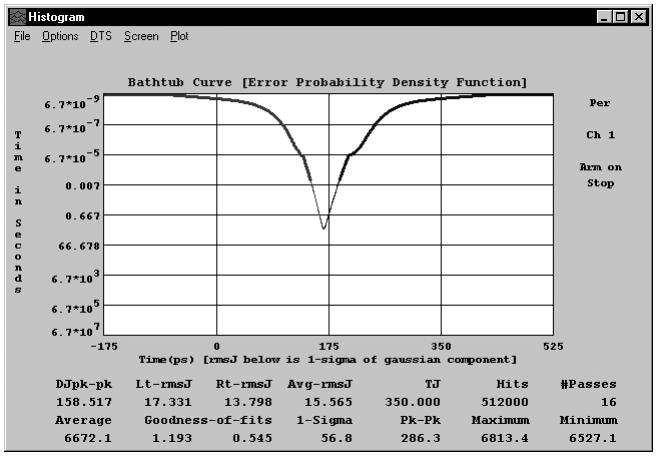
Modulation data in time and frequency domain

New TailFit™



From Traditional Histogram...

To Reliability Modeling Plot.



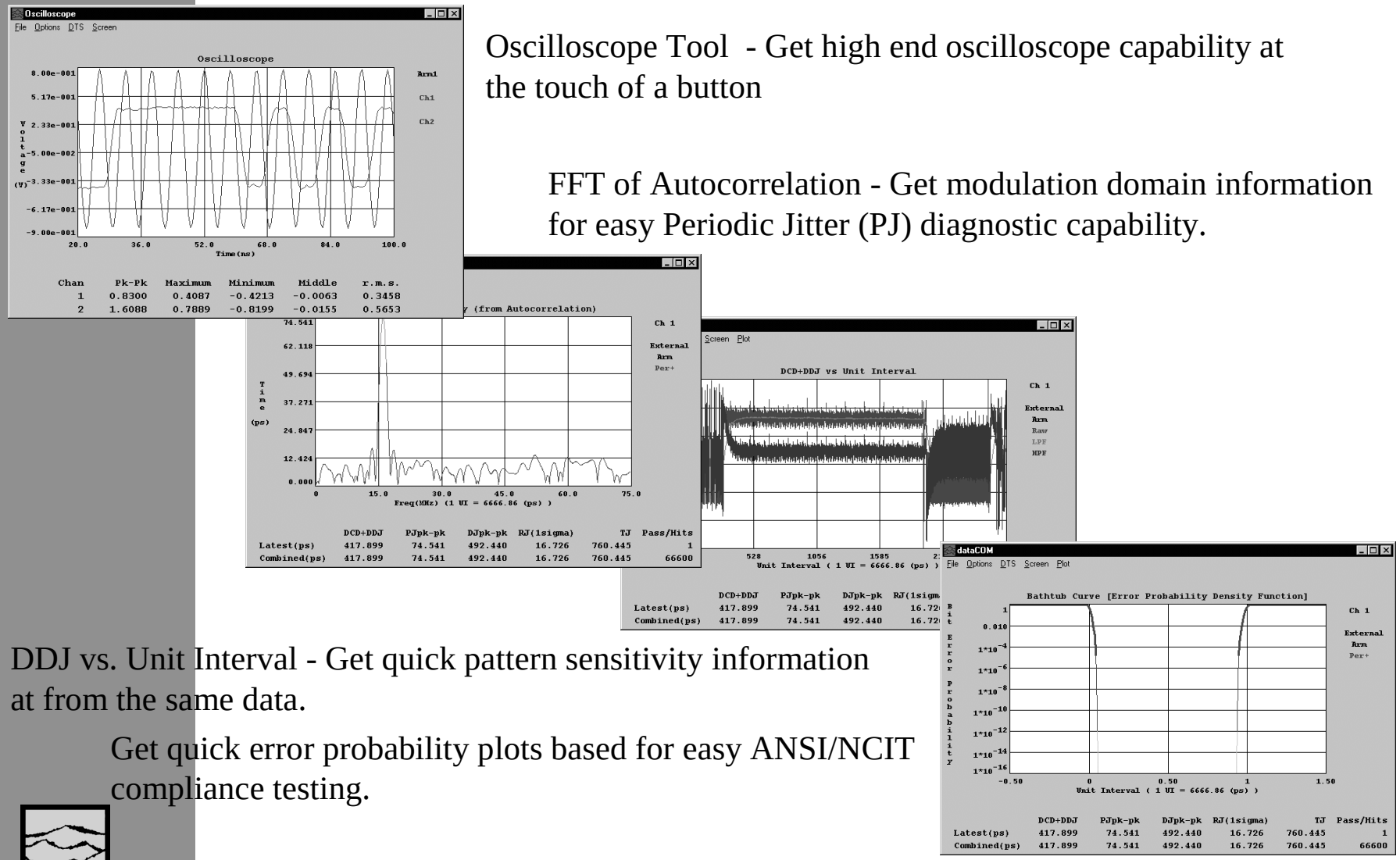
In one easy step.

Get the VISI advantage

dataCOM

- Analyze Jitter Components present on a data stream
  - Works great on random data
  - Separate jitter components over entire frequency band, or, apply internal band pass filters for specific frequency sensitivities.
- New TailFit™ algorithm enhances the accuracy of the dataCOM tool set
  - Get full MJS compliance testing without the use a bit clock.
- New Eye Histogram tool enables the user to analyze clock to data jitter effects
  - all the features of an Eye Diagram plus TailFit™ for expanded failure data.

dataCOM Tools



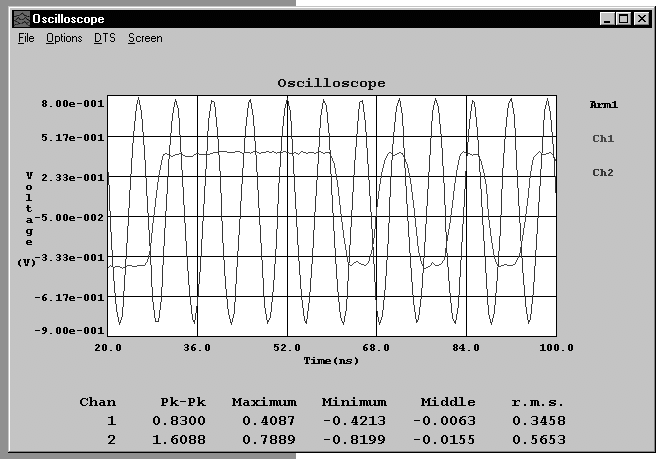
Oscilloscope Tool - Get high end oscilloscope capability at the touch of a button

FFT of Autocorrelation - Get modulation domain information for easy Periodic Jitter (PJ) diagnostic capability.

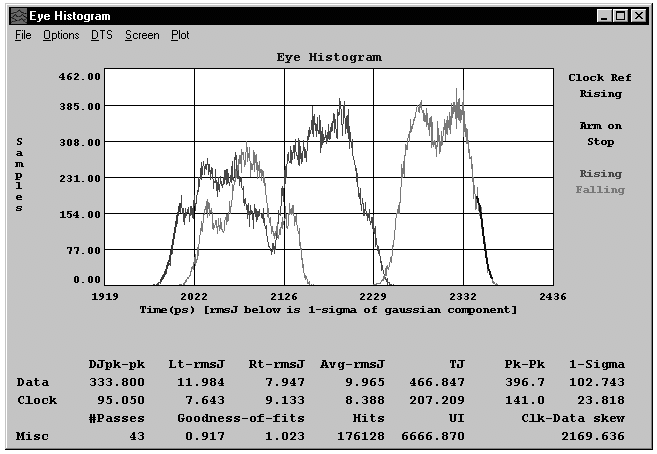
DDJ vs. Unit Interval - Get quick pattern sensitivity information at from the same data.

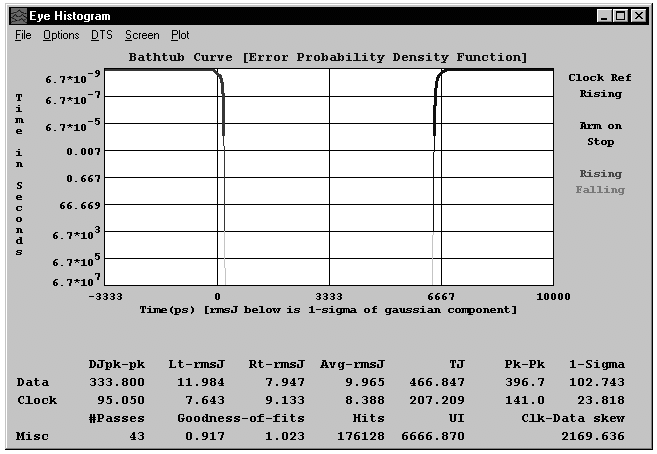
Get quick error probability plots based for easy ANSI/NCIT compliance testing.

New Eye Histogram Tool



From Scope Picture to Rising Edge/Falling Edge Distribution Plot to Error Probability Plot in one easy step.

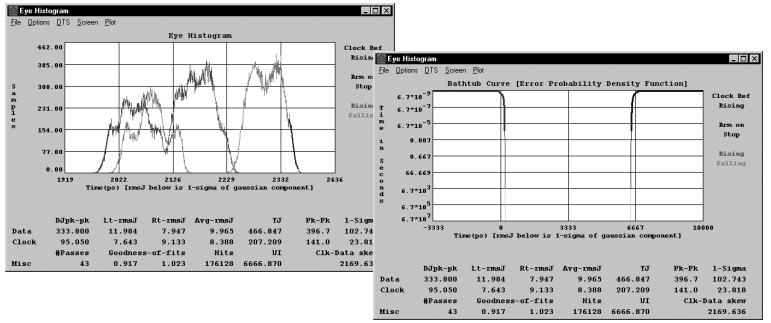




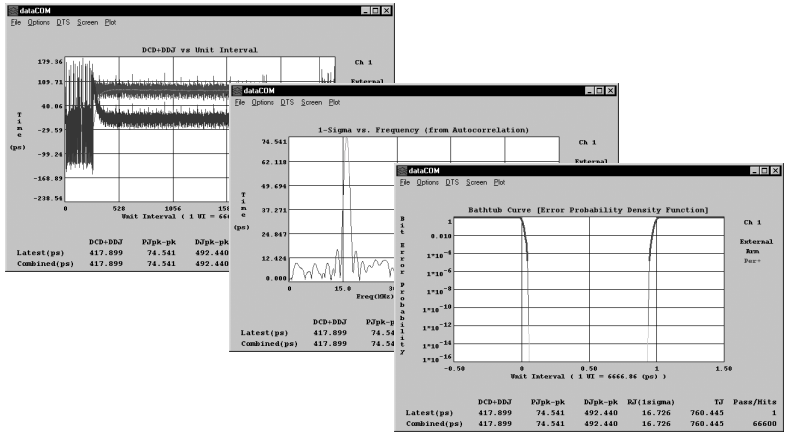
How do the VISI tools work?

What are the dataCOM tools?

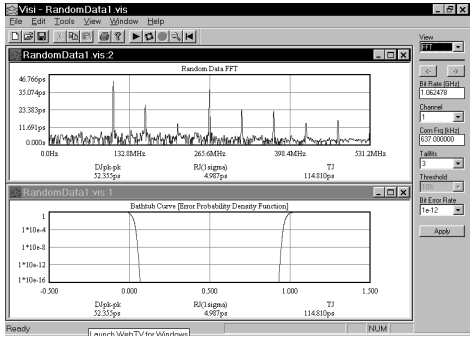
- Eye Histogram
  - Analyzes “Clock to Data” Jitter



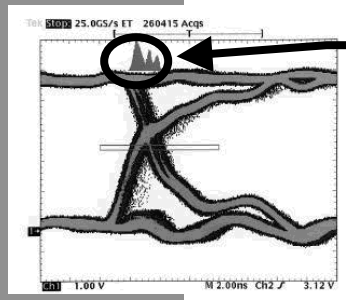
- dataCOM
  - Analyzes jitter on JUST the data



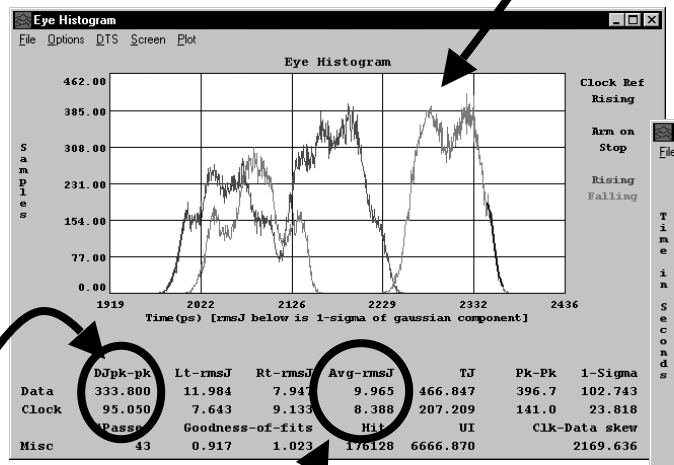
- Random Data Tool
  - Analyze jitter on data without any knowledge of the data stream
  - Analyze jitter on live networks, active Fibre Channel links and scrambled disk drive data.



A new look at Eye Diagrams

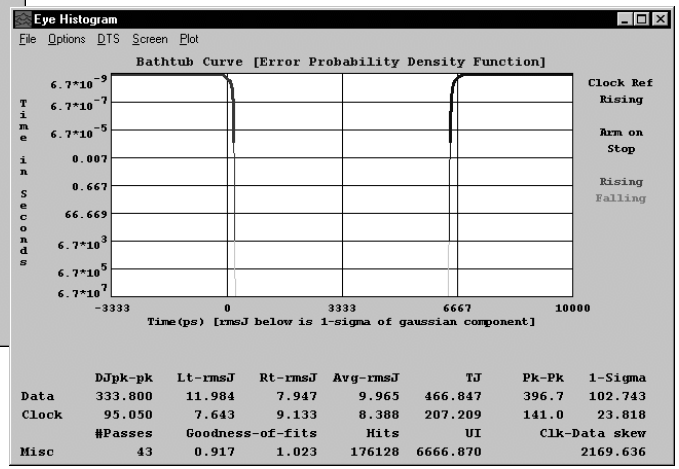


Total Measurement Histogram



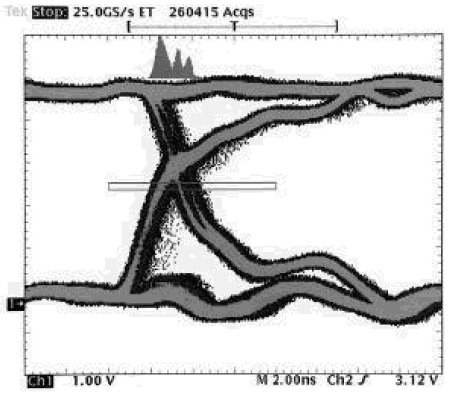
RJ/DJ separation and TJ calculation of clock and clock-data

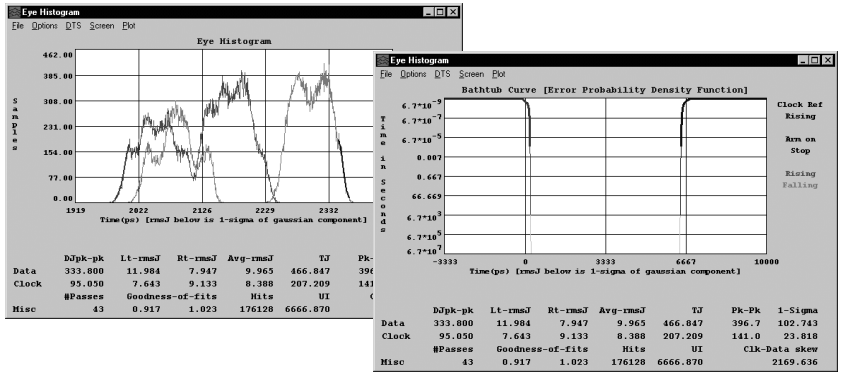
Bathtub curve of histogram data for complete reliability modeling



- Eye Histogram Tool takes traditional Eye Diagram to a new level
  - Same “Clock to Data” Jitter as the other tools.
  - No trigger delay
  - DJ/RJ separation for easy calculation of TJ
  - Bathtub curve for easy correlation with BERT.
  - Analyze Rising Edges separate for Falling Edges.

Eye Diagram vs. Eye Histogram

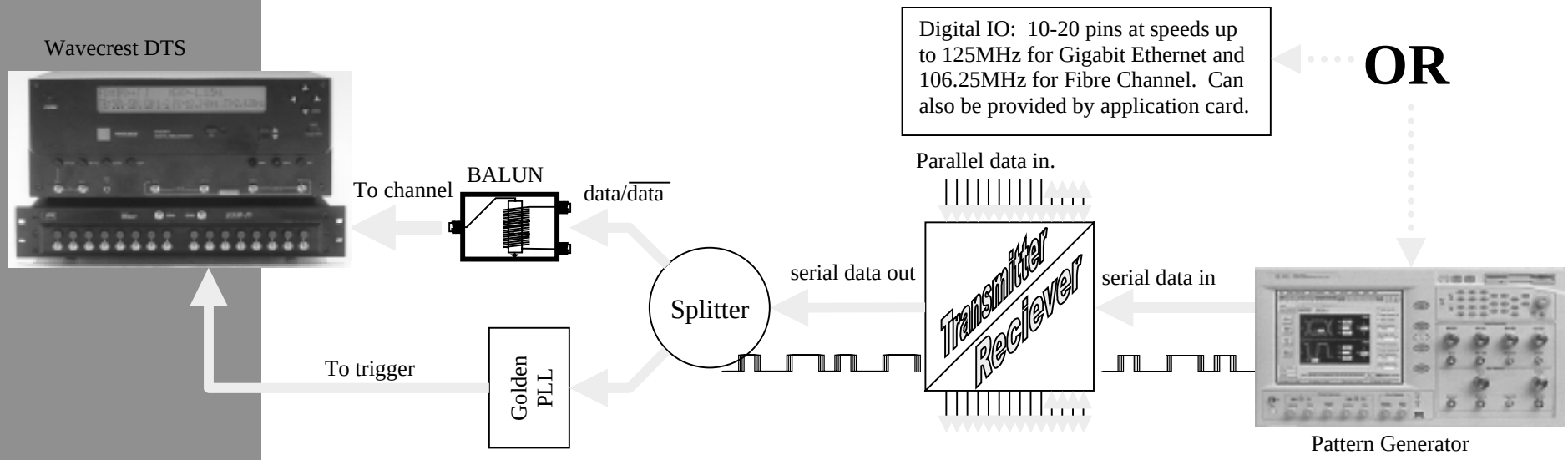




- Eye Diagram is ideal for voltage vs. time analysis
  - Use Eye Diagram for verifying voltage level stability, over shoot ringing, and other voltage based measurements
- Not a good tool for Jitter Measurement
  - No Jitter Separation
  - TJ estimate of clock to data jitter takes several hours to accumulate enough data to make a proper estimate
  - Not ANSI compliant.

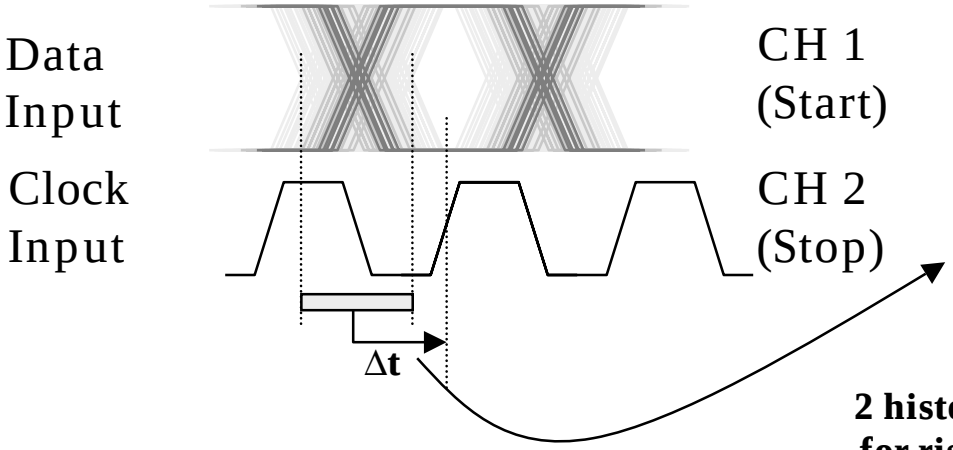
- Eye Histogram gives great jitter information
  - DTS is a Time measurement instrument, therefore, time measurement is second to none.
  - VISI algorithms give complete RJ / DJ separation for accurate reliability modeling AND ANSI compliance testing.
- Eye Histogram is not an Oscilloscope.
  - Use VISI Oscilloscope Tool for voltage vs. time relationship

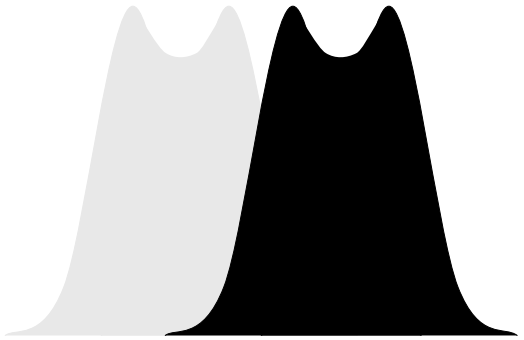
Equipment Setup of Eye Histogram



- Set up is the same as an Oscilloscope Eye Diagram
  - Use compliant PLL as clock source (just as in o'scope) for better frequency response modeling
  - No need for delay lines (DTS does not have a trigger delay)
  - Use BALUN and 50% threshold crossing as channel input.
- Clock signal is connected to channel 2 and data signal is connected to channel 1
  - This results in a data to clock measurement.

How is the Measurement Made?



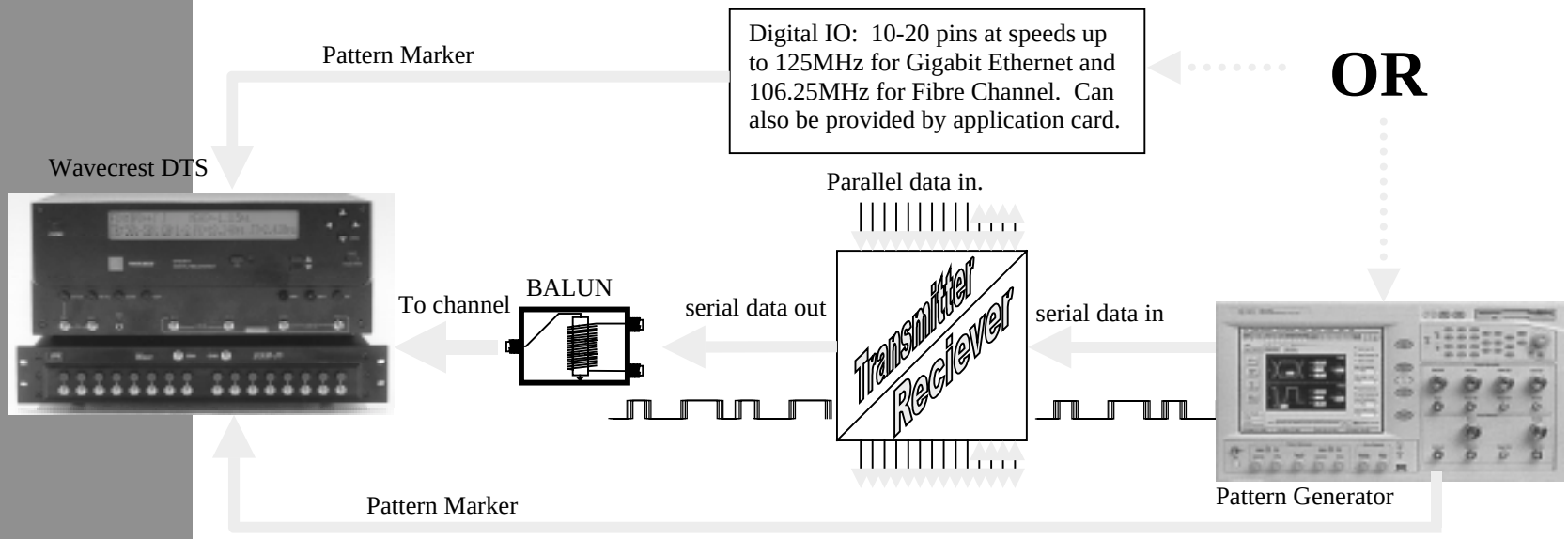


2 histograms of Δt measurements. One for rising edges, one for falling edges.

- Selecting the "real" measurements
  - The tool automatically eliminates any time measurements which exceed one bit period (just as the scope does)
  - Be careful when correlating with o'scope. Most o'scopes have a trigger delay that forces the user to look at the wrong data histogram.
- Skew of histograms indicates asymmetric cross point.
  - Rising Edge Histogram before Falling Edge Histogram indicates cross point is below starting trigger level.
  - Falling Edge Histogram before Rising Edge Histogram indicates cross point is above starting trigger level

(Eye Histogram is basically a t_{PD} measurement with built in data filters.)

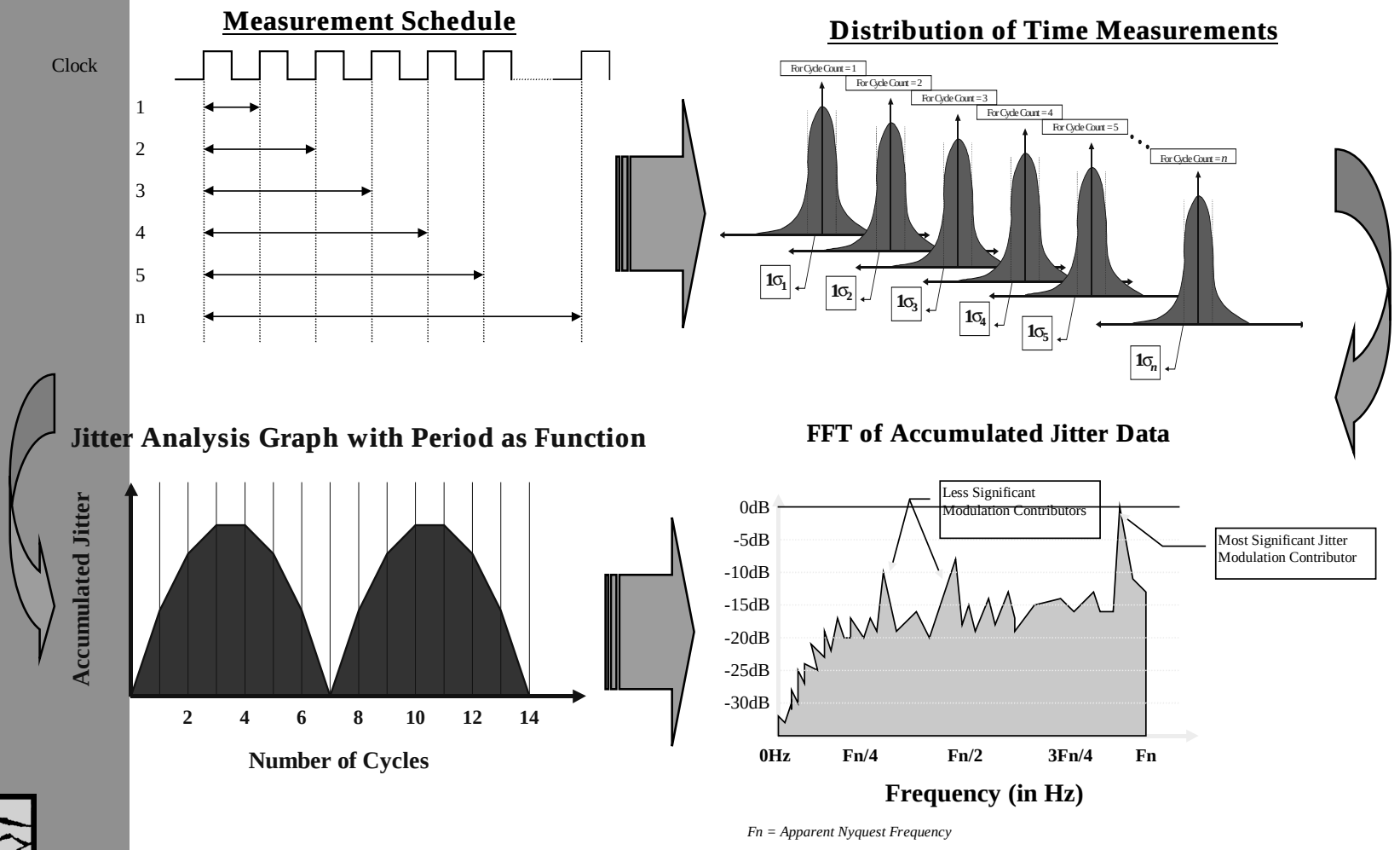
Jitter Measurements on ONLY data



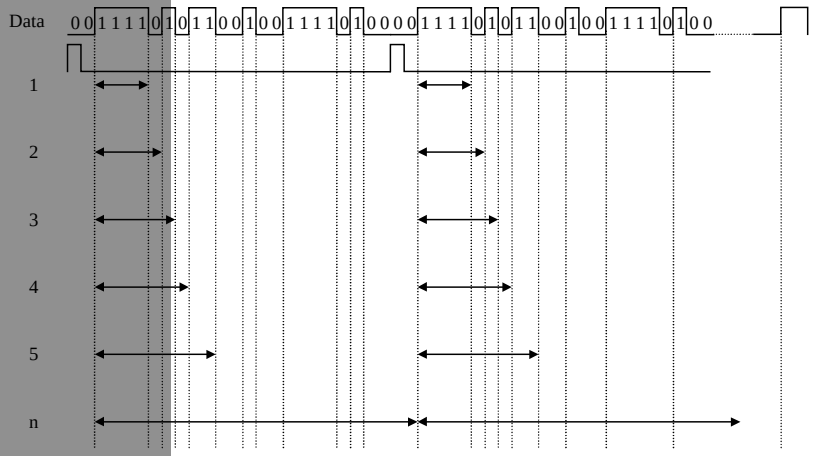
- Use Pattern Marker to optimize data dependant jitter separation.
  - Optimal accuracy is achieved when using pattern marker and TailFit™ on short patterns
- Use Balun and 50% Voltage level
- Data Plots include:
  - Data Dependant Jitter vs. UI (for pattern sensitivity testing)
  - Uncorrelated Jitter vs. frequency (for PJ detection)
  - Bathtub Curve (Eye Closure vs. BER)
- Based on patented Accumulated Time Analysis™ routine

The Math Behind VISI dataCOM Tools

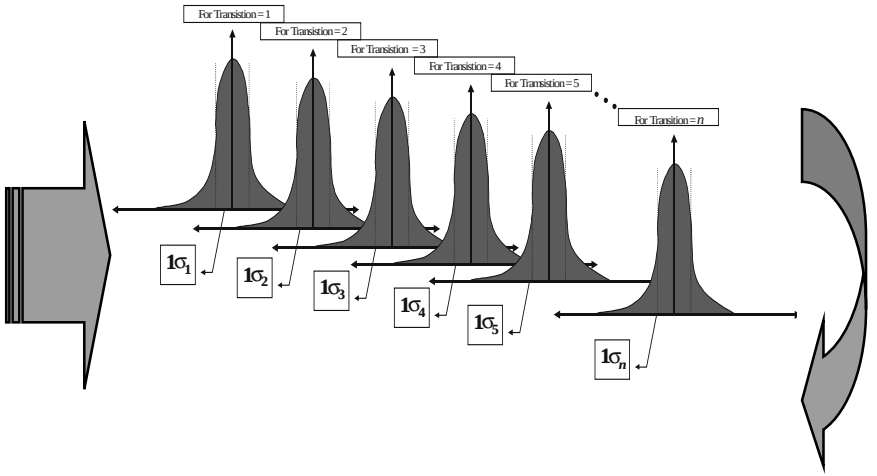
Review of Accumulated Time Analysis™

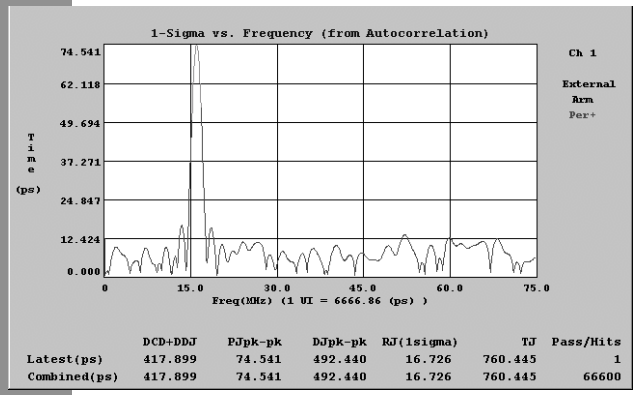


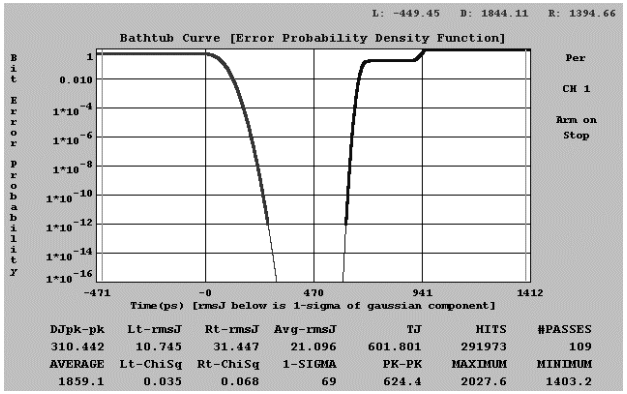
VI™ DataCOM Known Pattern & Pattern Marker - Theory of Operation



Transition Distributions







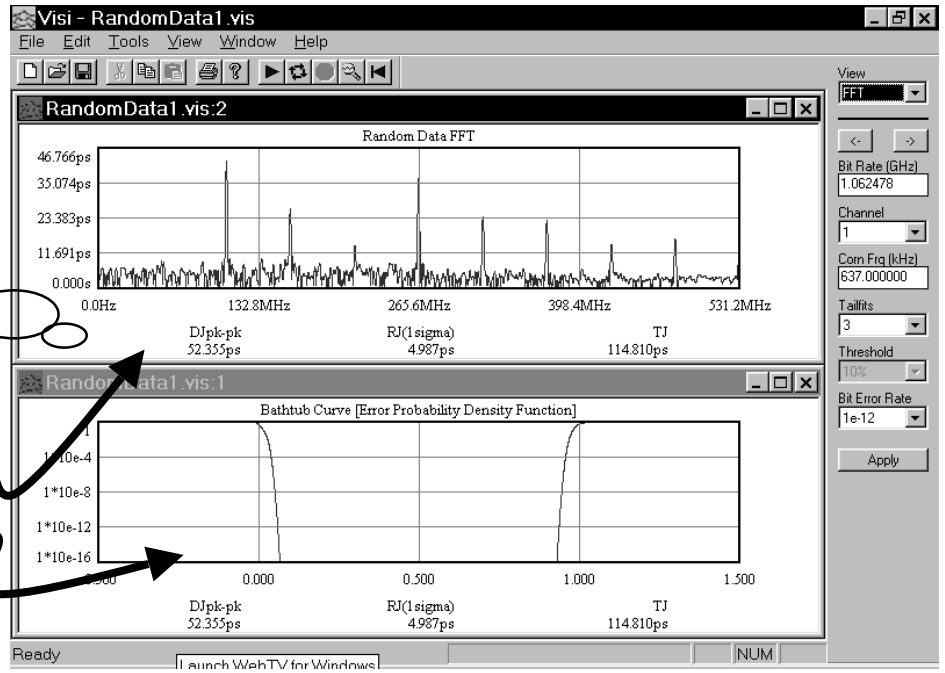
How do I Generate a Marker?

- Using Wavecrest's AGT100
  - Recover bit clock and perform pattern recognition for use with patterns with a header section preceding it
  - Count bit clock for pattern length trigger for patterns with constant length. (no random idles interleaved.)
    - User can program the length of the pattern or the bit stream to trigger on
  - Built in Balun
  - Built in linear amplifiers for low swing signals

Random Data Tool

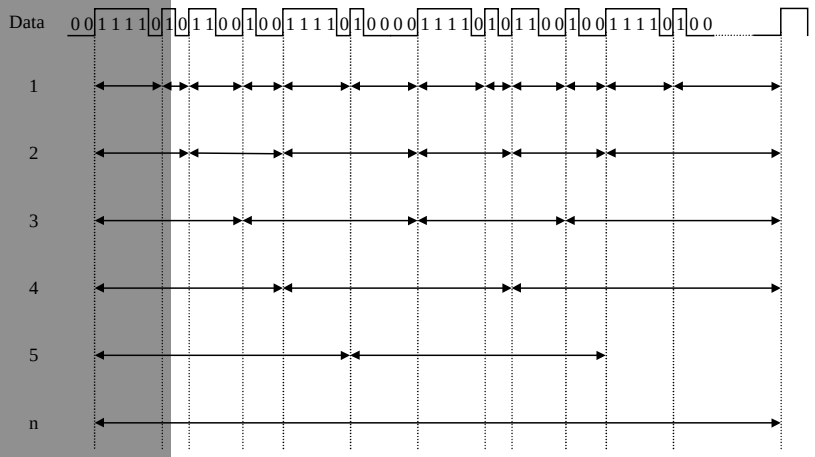
This is the first tool featuring User Friendly Controls. Watch for VISI 6.0 which will feature this capability in all tools!

Jitter Frequency Plot and Bathtub Curve all without any knowledge of the pattern

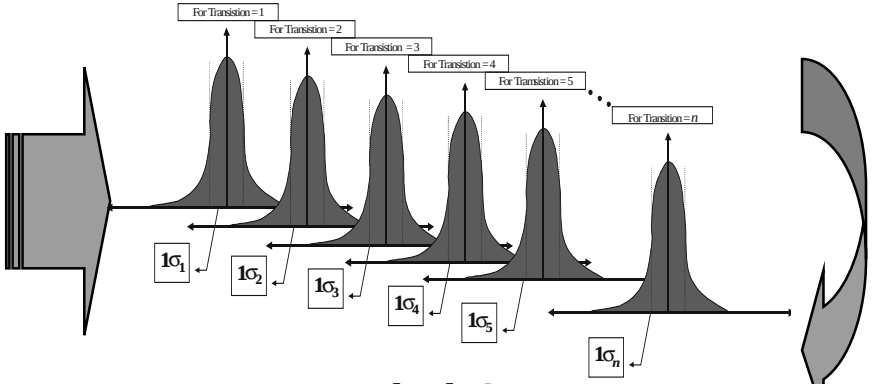


- Based on random data streams, Random Data Tool lets the user analyze any data stream with no marker, bit clock nor knowledge of the pattern.
- Uses TailFit™ algorithm and special sampling technique to look at fully random data streams.

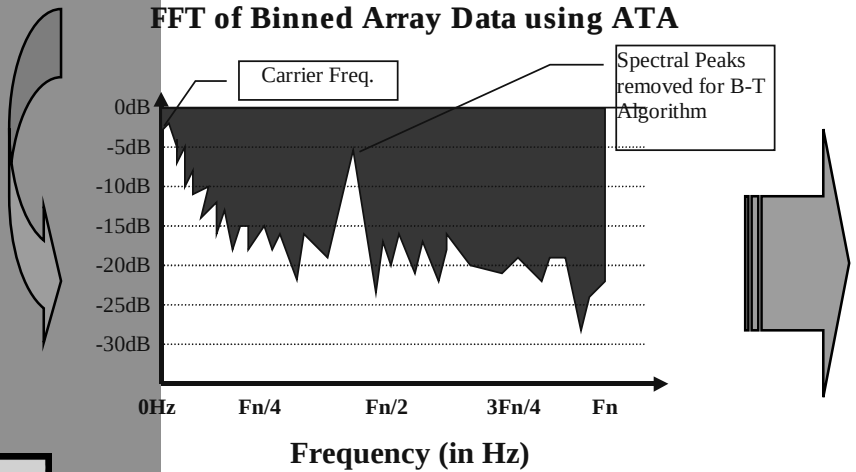
VI™ DataCOM Random Pattern Theory of Operation



Measurements Binned to Closest UI Boundary

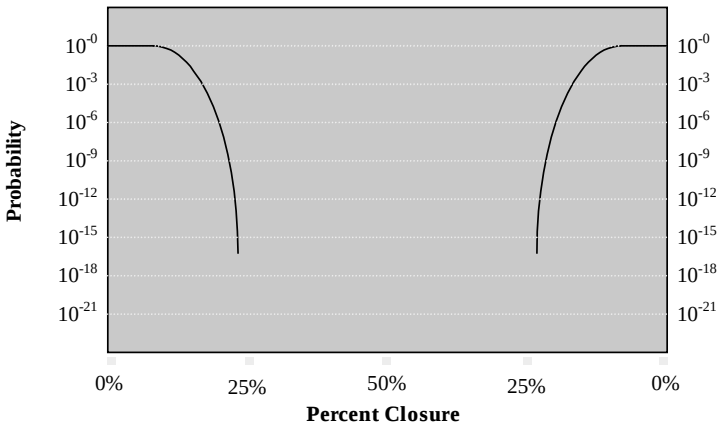


FFT of Binned Array Data using ATA

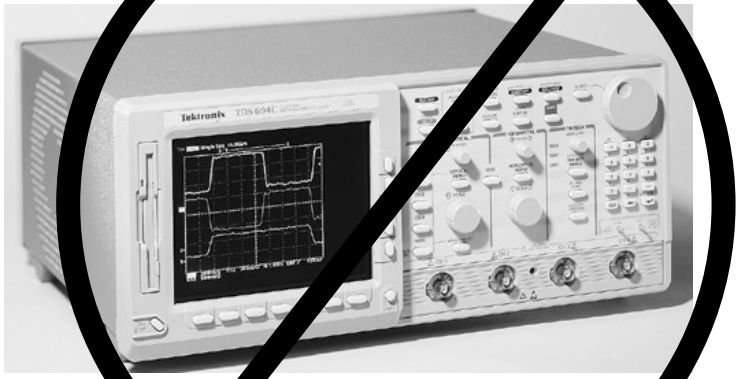


Fn = Apparent Nyquest Frequency

Bathtub Curve
(Probability versus Percent Closure)

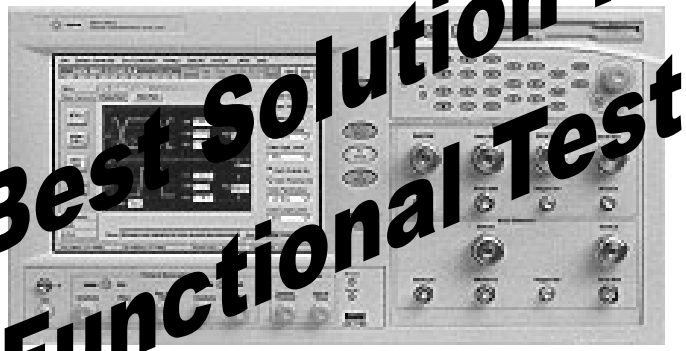


Jitter Output Testing



Cannot use a Digitizing Oscilloscope

Best Solution for Jitter Analysis



Best Solution for Functional Test

(with FC compliant CDR(Golden PLL) for triggering)

Best Solution for Waveform Analysis

(with FC compliant CDR(Golden PLL) for triggering)

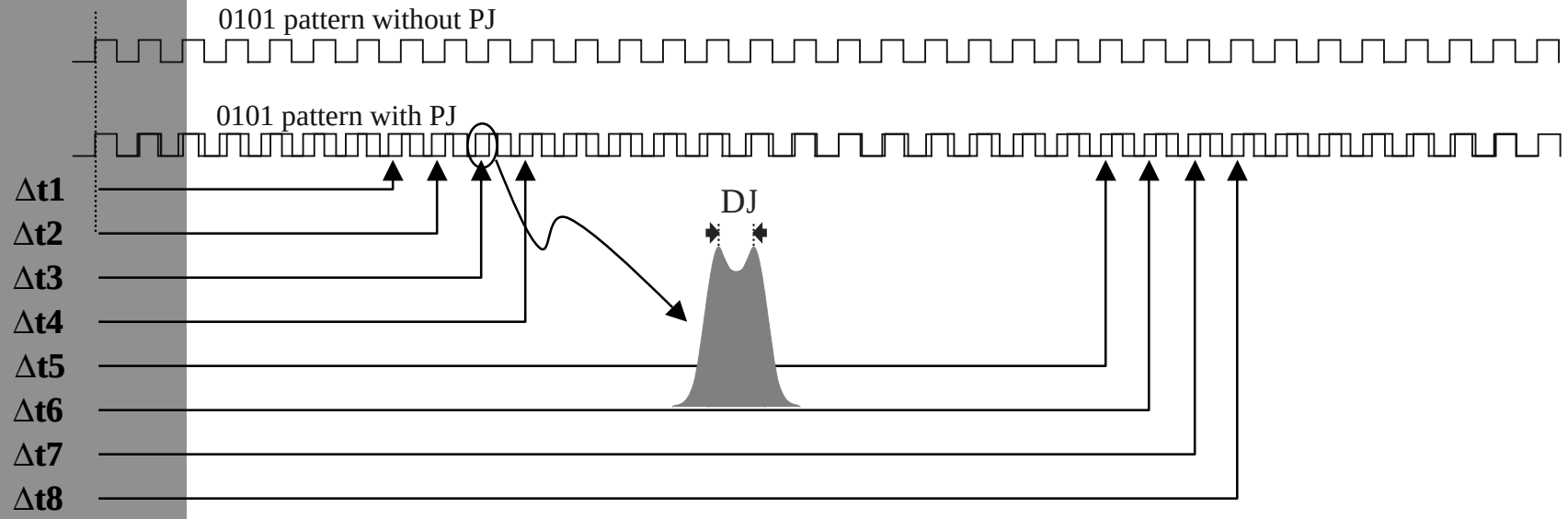
Jitter Transfer Testing

These are some helpful hints based on real world experiences from SONET testing. As you may know, Jitter Transfer has not yet been addressed by the MJS committee. These suggestions are included to provide insight into techniques for measuring Jitter Transfer with the Wavecrest Communication Signal Analyzers. Obviously, Other tools, such as SONET analyzers, already have this capability although their measurement time is quite long. Also, Wavecrest is continuing to develop solutions that improve ease of use.

Jitter Transfer Testing

- Use Pattern Marker when analyzing data.
  - Can also use clock stream in which case, no pattern marker is necessary.
- Use BALUN or DSM16D for differential signal support.
  - DSM16D is a 4GHz Bandwidth, 8D:2SE matrix.
- Signal summation could be done with matched dividers or through internal power summation of instrumentation.
  - Some models of pattern generator and noise source have signal inputs which can be used to sum signals.
- Use DTS to analyze the input signal to adjust Noise and Modulation source to desired amplitude.
- Noise Source not necessary for SONET Jitter Transfer testing.

Measuring Jitter Transfer

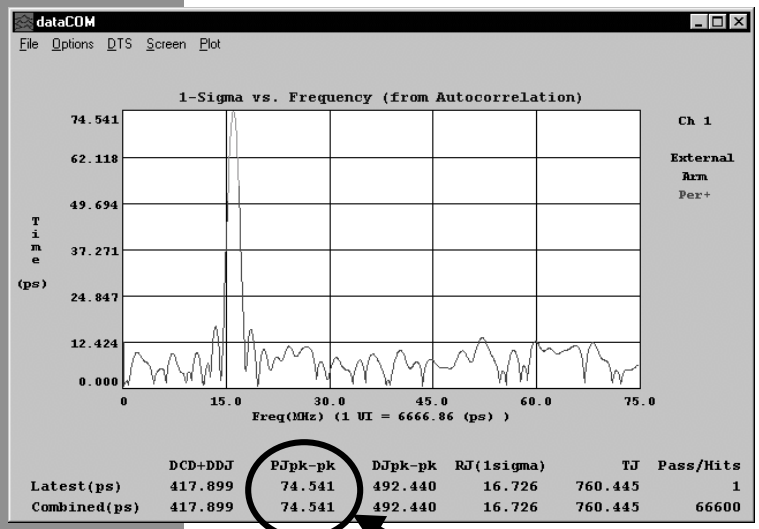


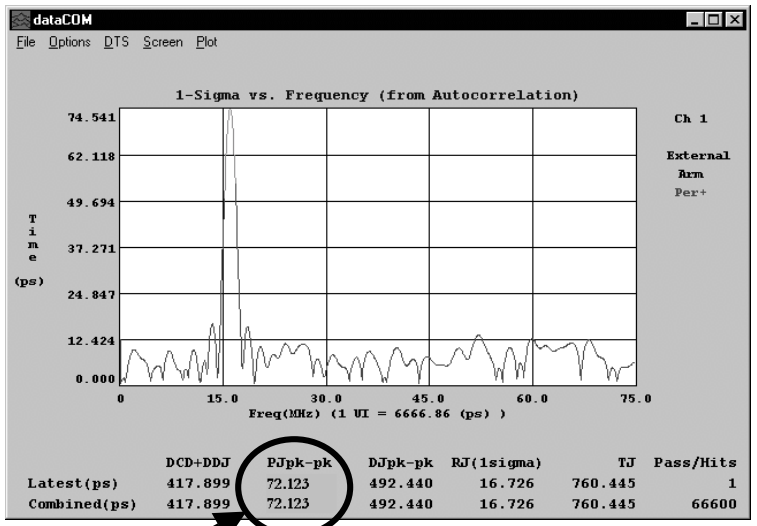
- Measure elapsed time and analyze the jitter for accumulated periods of [FC / (2*FM) ±2]
  - The "±2" is to account for inaccuracy of modulation source
- Find the maximum DJ for Δt1-4 and Δt5-8. Average the max values. (can also use pk-pk of the distribution for faster results)
  - Two groups are used to account for measurement repeatability.
- Then, compare the DJ going into the device to the DJ coming out using the gain equation:

$$\text{Gain} = 20 \log(DJ_{OUT} / DJ_{IN})$$

- Perform this test for several frequencies.

Using VISI for Jitter Transfer

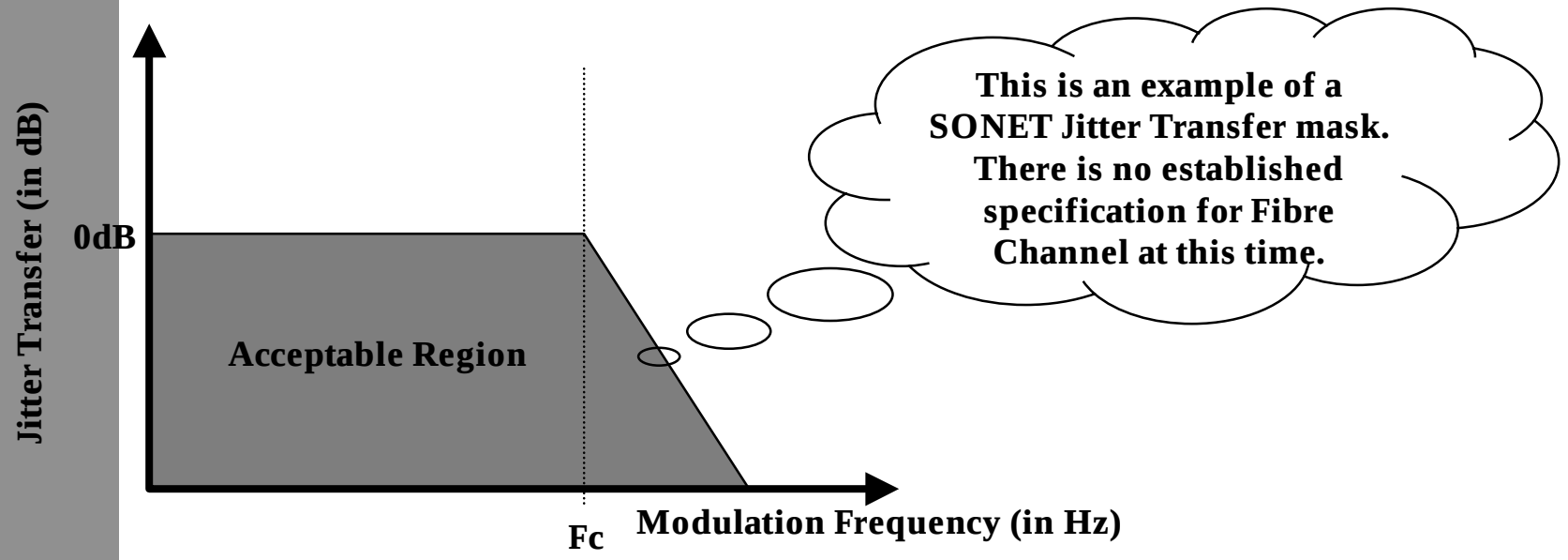




Compare these two numbers with Gain Equation

- Using VISI, measure $PJ_{pk\text{-}pk}$ on the input and the output of the device of system.
- Use this technique for analyzing Jitter Transfer on data streams or clock-like patterns.
- Can also be done in GPIB commands for automated laboratory programming environments (LABVIEW).

Jitter Transfer Specifications

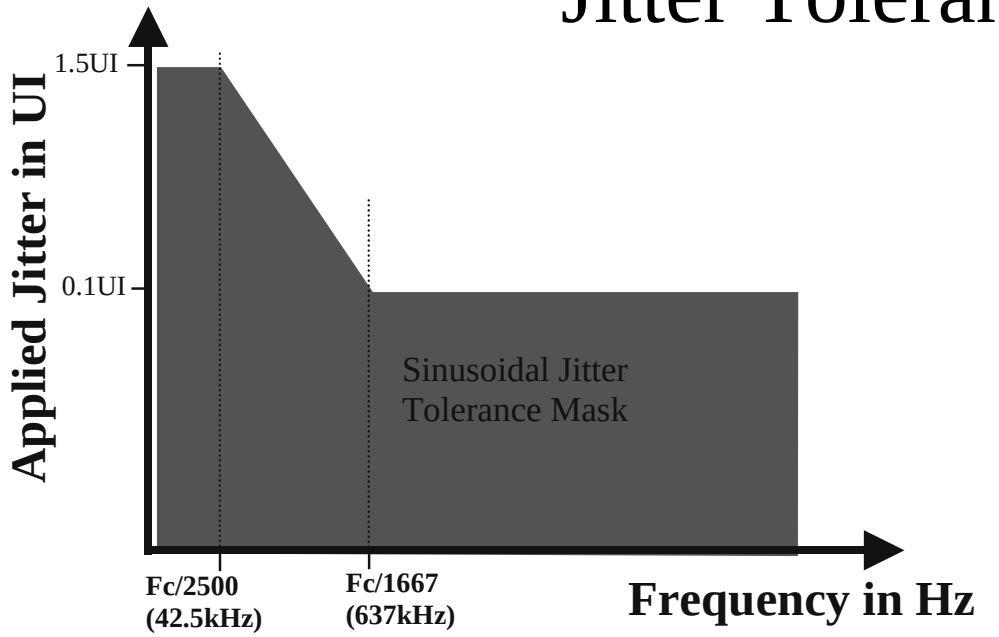


JITTER TRANFER –

The ratio between the jitter output and jitter input for a component, device, or system often expressed in dB. A negative dB jitter transfer indicates the element removed jitter. A positive dB jitter transfer indicates the element added jitter. A zero dB jitter transfer indicates the element had no effect on jitter. The ratio should be applied separately to deterministic jitter components and Gaussian (random) jitter components. The concept of jitter transfer is not addressed in [MJS] document.

Jitter Tolerance Testing

Jitter Tolerance Testing



- Jitter Tolerance on Fibre Channel devices consists of applying prescribed amounts of non-sinusoidal DJ and RJ in conjunction a frequency sweep of sinusoidal jitter
  - Applying all components simultaneously tests the interaction of each jitter component.
  - Be sure to apply the correct amount for the given compliance point.h

Jitter Tolerance Specification

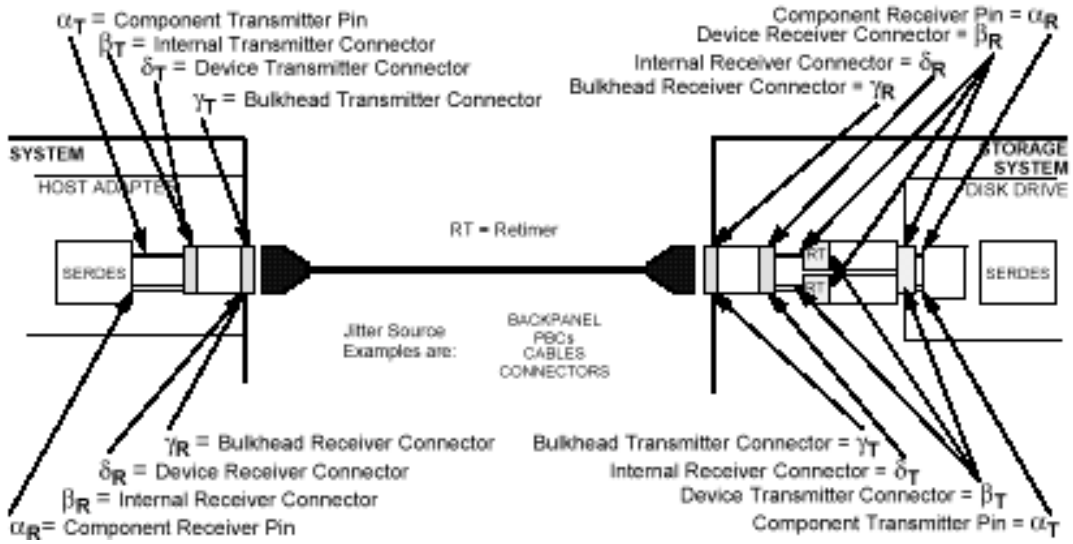
Table 7 – 1,0625 GBaud jitter tolerance allocation example

Variant	Jitter (Unit Interval - UI)								
	Component	α_T	β_T	δ_T	γ_T	γ_R	δ_R	β_R	α_R
100-SM-xx-x (single mode)	DJ	0,10	0,11	0,12	0,21	0,23	0,36	0,37	0,38
	Sinusoidal	0,10	0,10	0,10	0,10	0,10	0,10	0,10	0,10
	Total	0,31	0,28	0,30	0,48	0,52	0,66	0,68	0,70
100-Mx-xx-x (multi-mode)	DJ	0,10	0,11	0,12	0,21	0,24	0,36	0,37	0,38
	Sinusoidal	0,10	0,10	0,10	0,10	0,10	0,10	0,10	0,10
	Total	0,31	0,28	0,30	0,48	0,52	0,66	0,68	0,70
100-xx-EL-x (copper)	DJ	0,10	0,11	0,12	0,13	0,35	0,36	0,37	0,38
	Sinusoidal	0,10	0,10	0,10	0,10	0,10	0,10	0,10	0,10
	Total	0,31	0,33	0,35	0,37	0,64	0,66	0,68	0,70

1. Note that the sinusoidal component of 0,10 UI is valid for frequencies of 637 kHz and higher. For frequencies below 637 kHz, the magnitude of the sinusoidal component must meet figure 9.
2. Although the jitter output corner frequency and jitter tolerance frequency maybe the same as detailed in this recommendation, it is recommended that the jitter tolerance corner frequency be greater than the jitter output corner frequency.
3. α_T, β_T, δ_T and γ_T are included to indicate that the jitter test signal can be injected at any point in the system to test the α_R point's jitter tolerance.

This implies a total RJ component .22UI or .0157UI (1σ)

α_R is made at the component of the receiver.

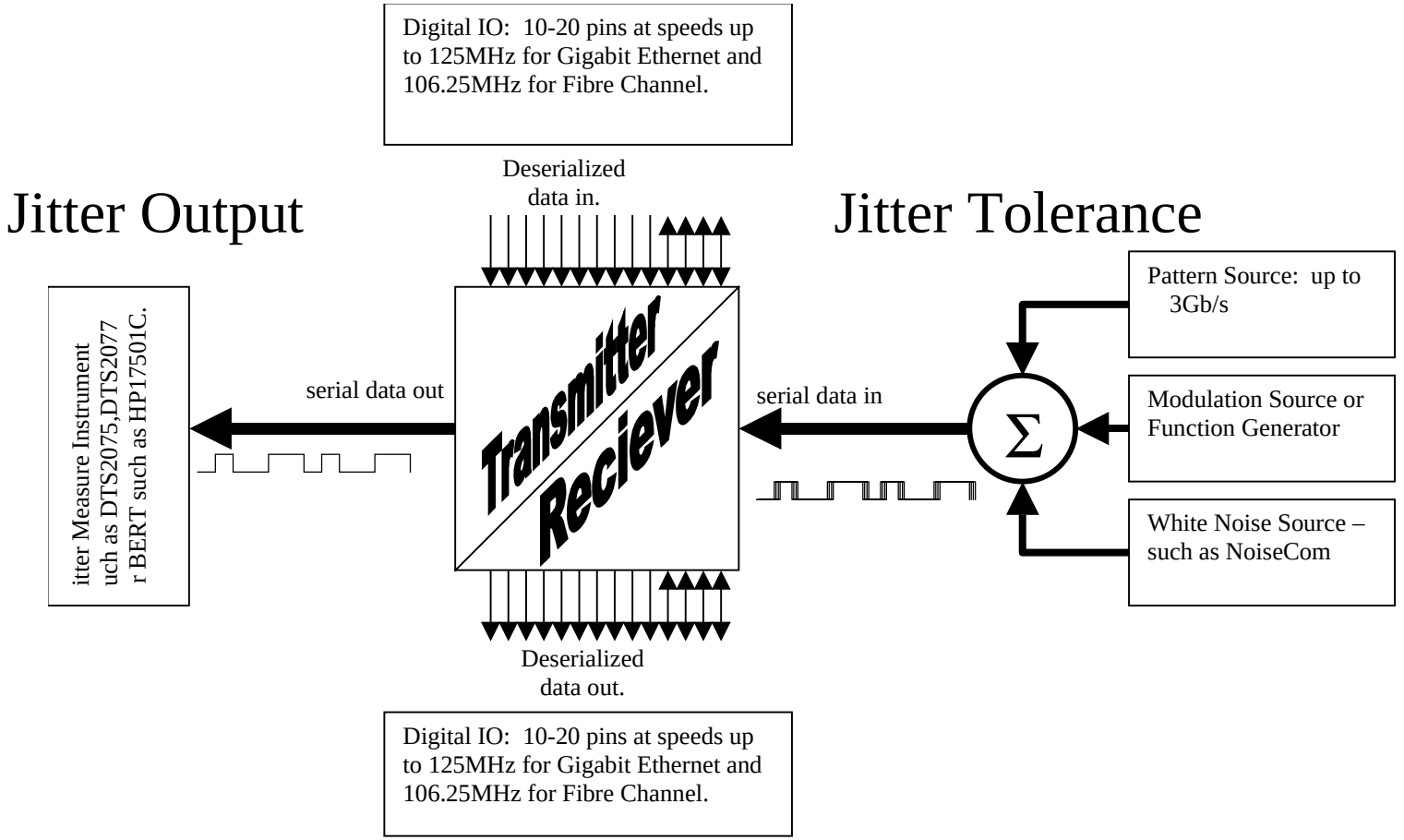


MJS Recommended Setup

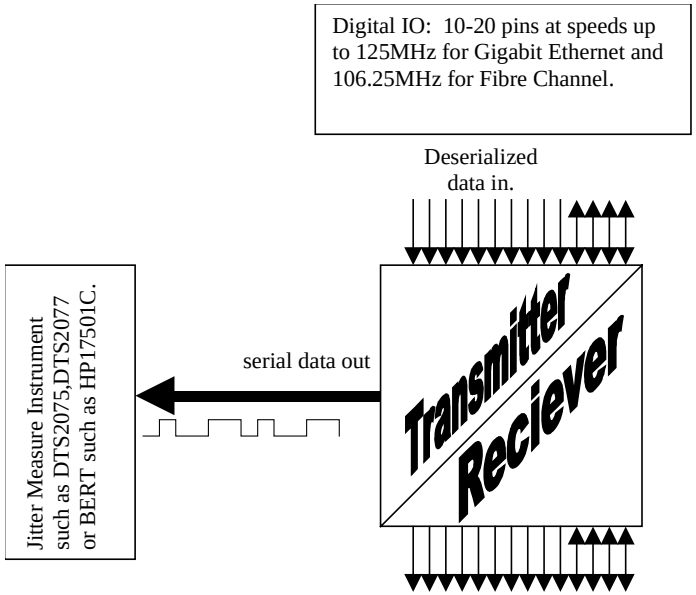
Use the DTS to verify the amplitude of the jitter components being applied.

Figure C.4 – Example of Jitter Test Setup for 10-bit SerDes

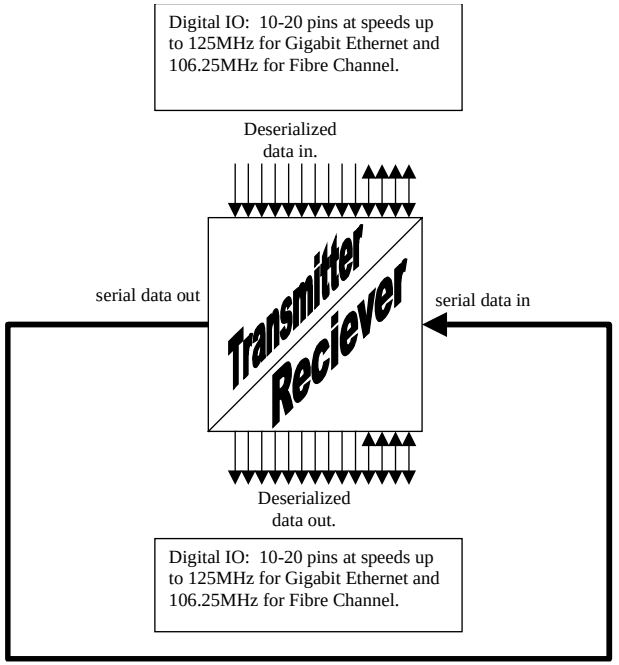
Fibre Channel and Gigabit Ethernet Complete Jitter Testing



Fibre Channel and Gigabit Ethernet Simplified Jitter Testing



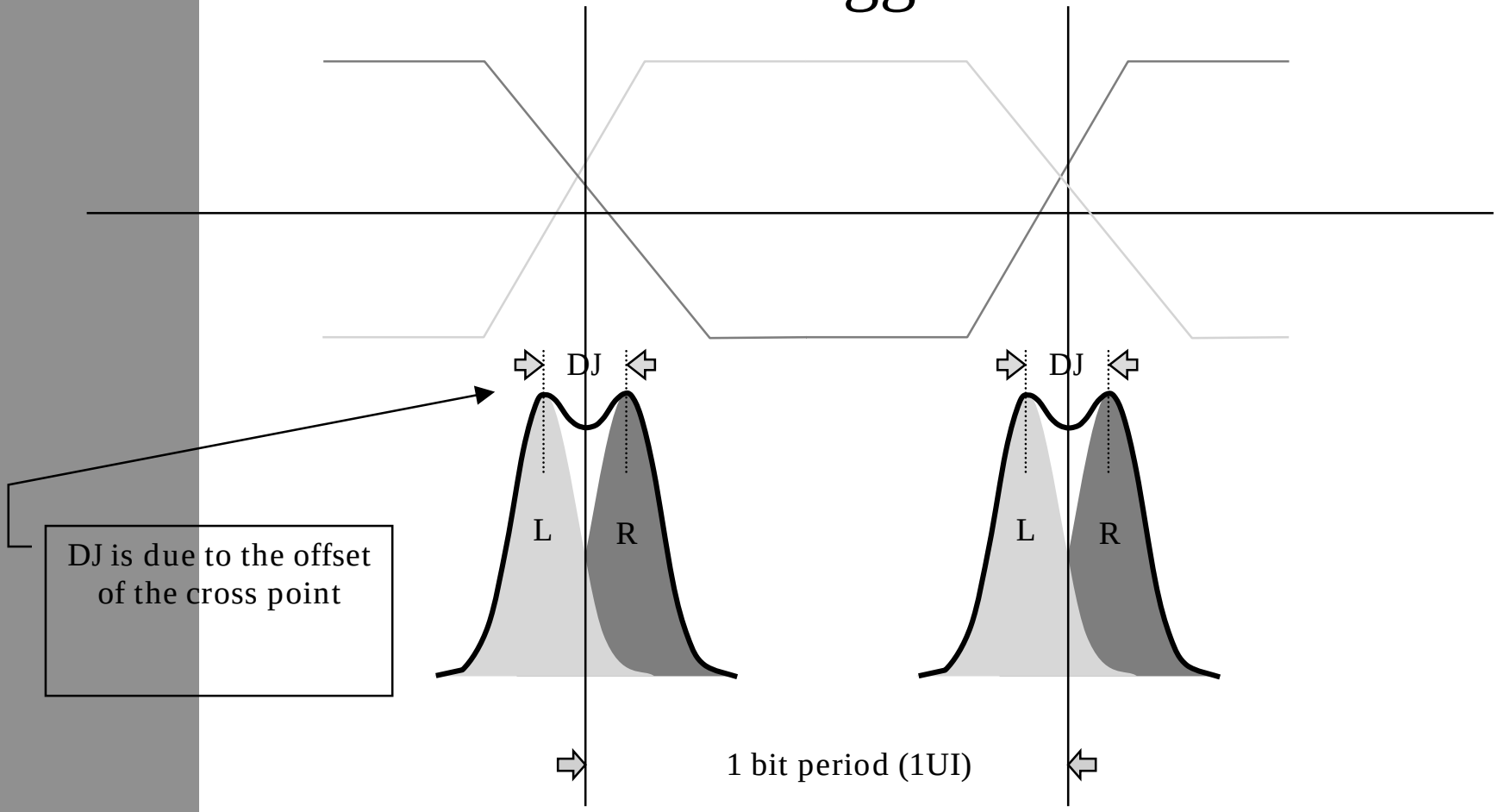
Jitter Output



Receiver Port Testing

Proper Measurement Techniques – Jitter Output (Generation)

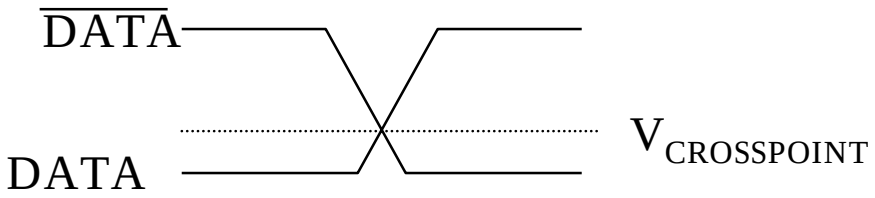
Where Should I trigger the Measurement?



- You must measure at the 50% point and you must use a BALUN.
- The 50% point is indicative of the point in time when the two complimentary signals are equal in voltage and thus best represents the point at which the differential receiver switches.

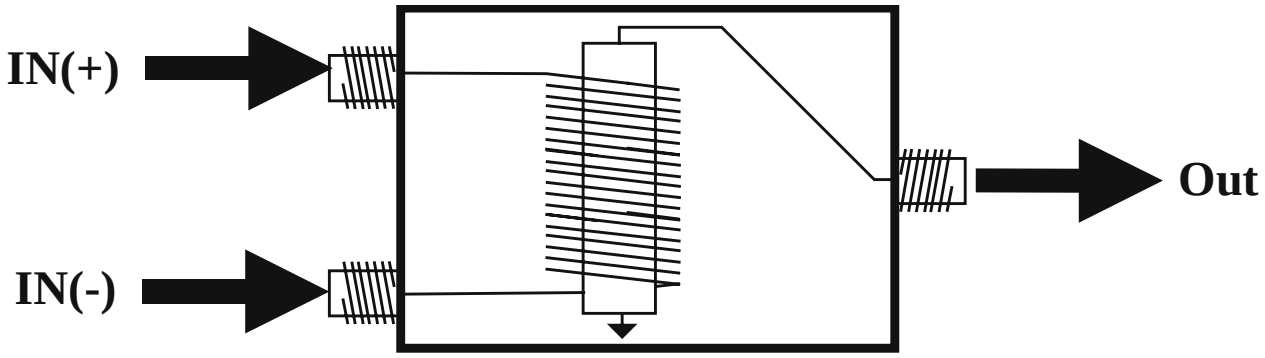
Measuring Differential Signals

- High Frequency Differential Signals Need Special Attention
  - Rise time and fall time for a given device are typically not equal.
  - Differential Input pins (receivers) typically transition when the two complimentary signals are transitioning through the same voltage. This voltage is called the crosspoint voltage and is depicted here.



- Jitter Measurements and Propagation Delay measurements must be taken from the crosspoint reference.
  - Since Differential Input pins use the crosspoint as the transition indicator, it is imperative that all time measurements be made from this point.
  - This is best done by using a balun

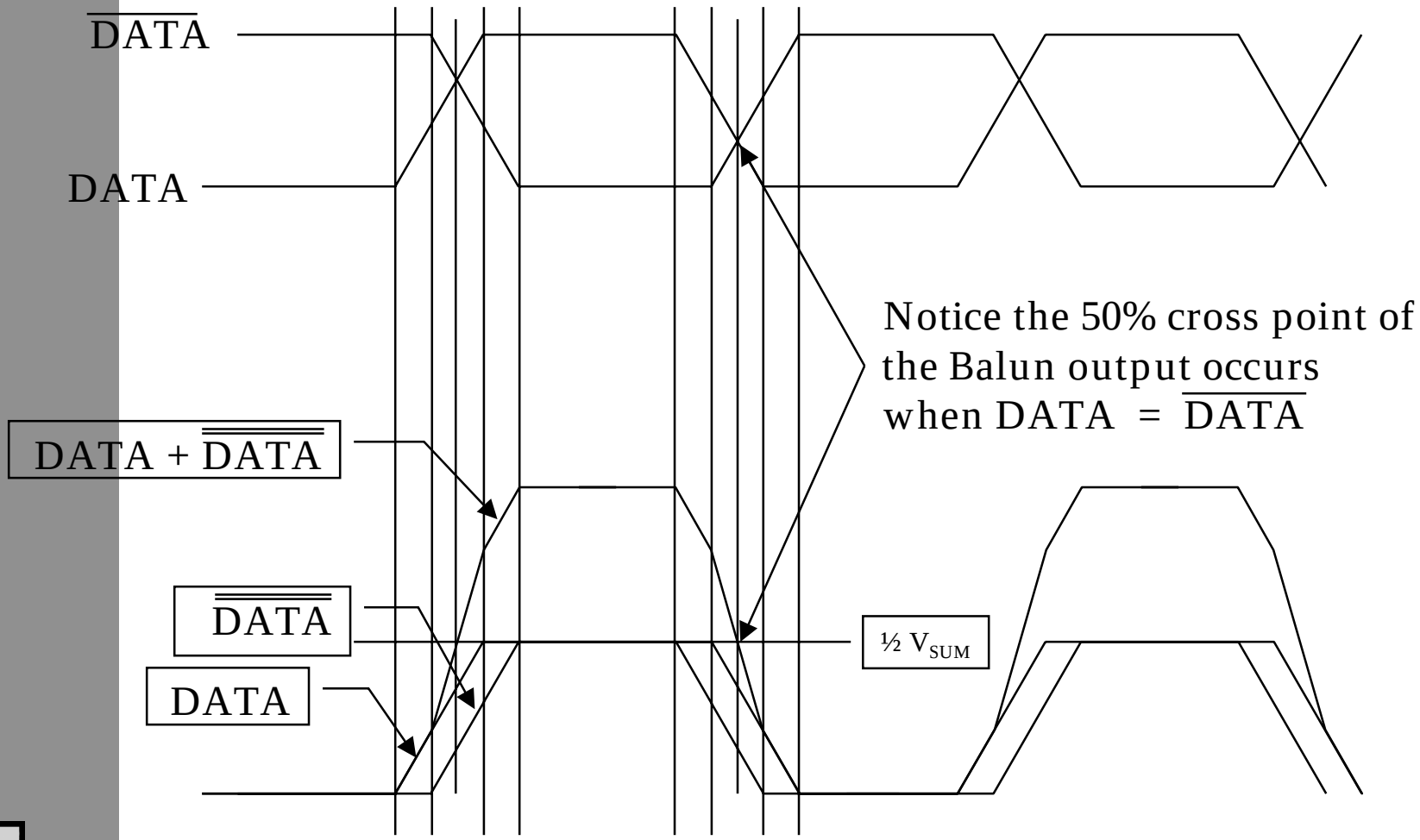
What is a Balun?



- Balanced to Unbalanced Converter (BALUN)
  - Used to convert differential signals to single ended using linear components.
  - Uses simple wound core architecture to convert differential signal single ended.
  - The output of the BALUN is AC coupled.
  - Permits high performance time measurements to be made by generating a single ended signal that has the same timing criteria as the original differential stimulus.
  - Single ended signal is a mathematical equivalent to:

$$Out = IN(+) - IN(-)$$

Understanding Balun Devices



Wrap-up

- Jitter Components are best analyzed with Jitter Tools
  - Must be able to separate RJ, PJ and DDJ
  - Must be able to quantify the amplitude and frequency of the jitter
- Every Tool has it's place
  - Use BERT for functionality testing
  - Use Scope for waveform verification
  - Use Wavecrest DTS for timing and jitter analysis
- Be sure to visit our web page for the latest material concerning Communication Signal Analysis

www. wavecrest.com

- Questions?

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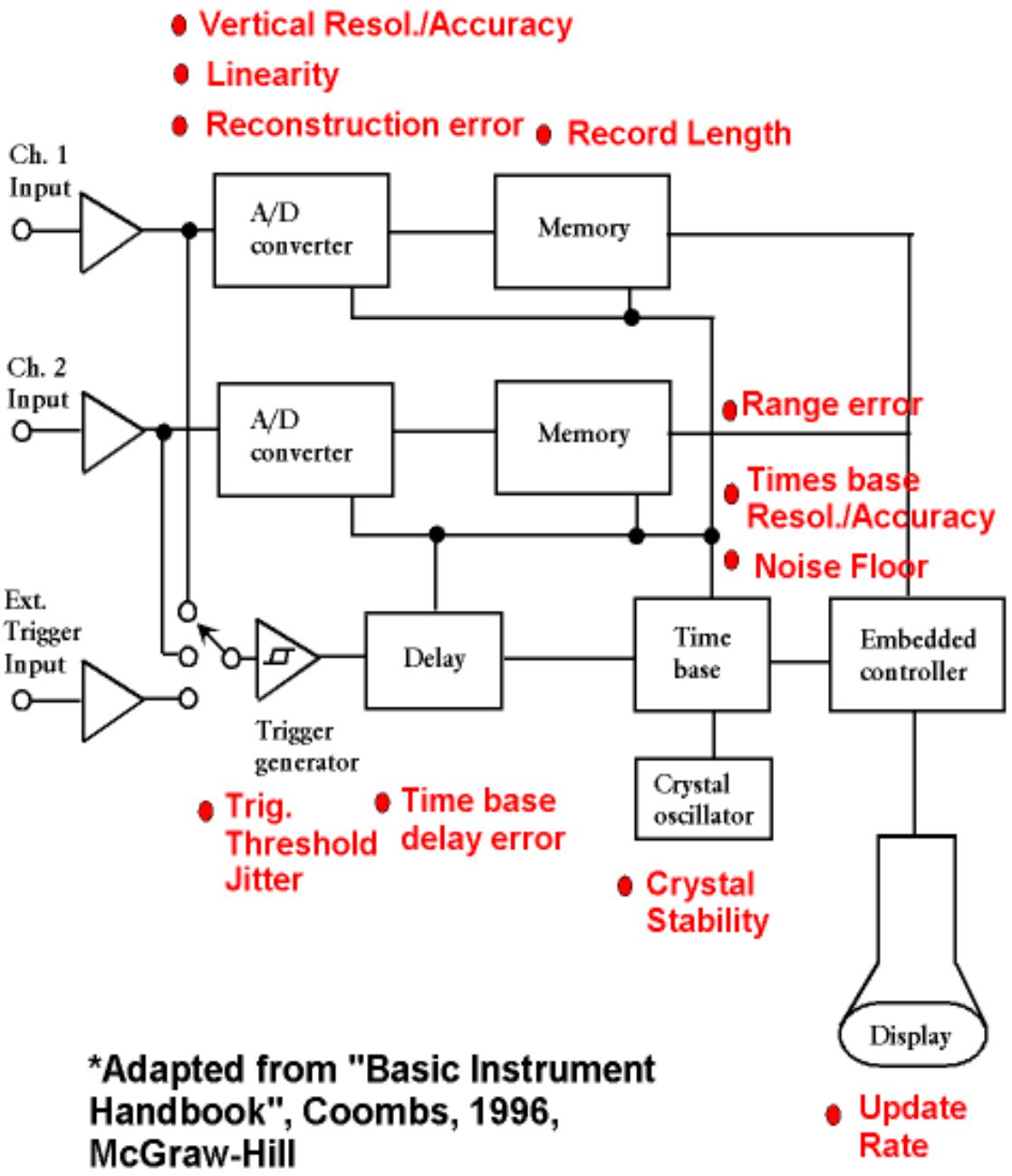
APPENDIX A

AVAILABLE EQUIPMENT

- DSO – Digital Sampling Oscilloscope (one-shot/repetitive)
- TIA – Time Interval Analyzer (MDA)
- BERT – Bit Error Rate Tester
- DTS-2070/2075 – Digital Time System
- Spectrum Analyzer
- ATE
- Custom

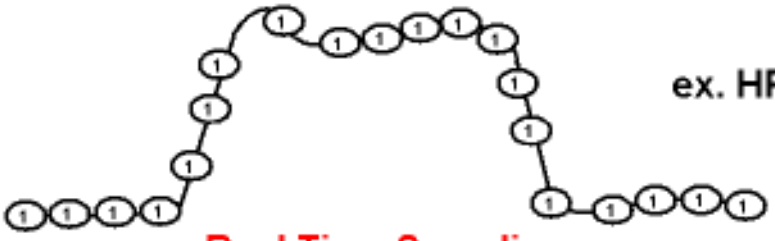
General Purpose Digital Sampling Oscilloscope

(key performance specifications)*



*Adapted from "Basic Instrument Handbook", Coombs, 1996, McGraw-Hill

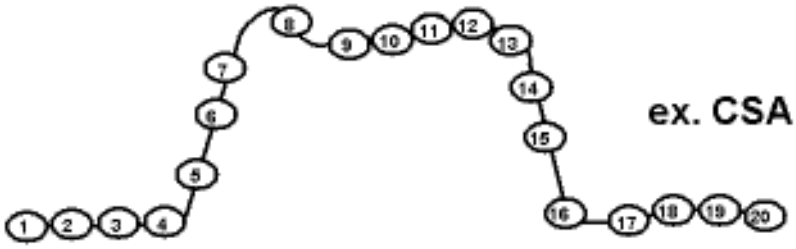
DSO Sampling Modes*



ex. HP54720D

Real Time Sampling

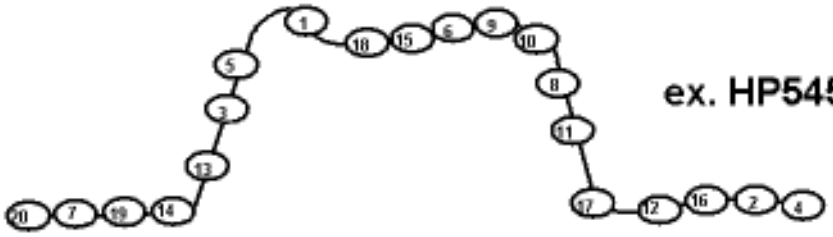
This sampling method captures entire waveform upon a single trigger event.



ex. CSA 803A

Sequential Repetitive Sampling

This sampling method acquires a new sample at a certain time interval after the trigger. Instrument increases this time delay by a fixed amount after each sample.



ex. HP54520C

Random Repetitve Sampling

Similar to Sequential Sampling except that the time difference between the trigger point and the sample point is random. Sampling is done constantly not waiting for a trigger event.

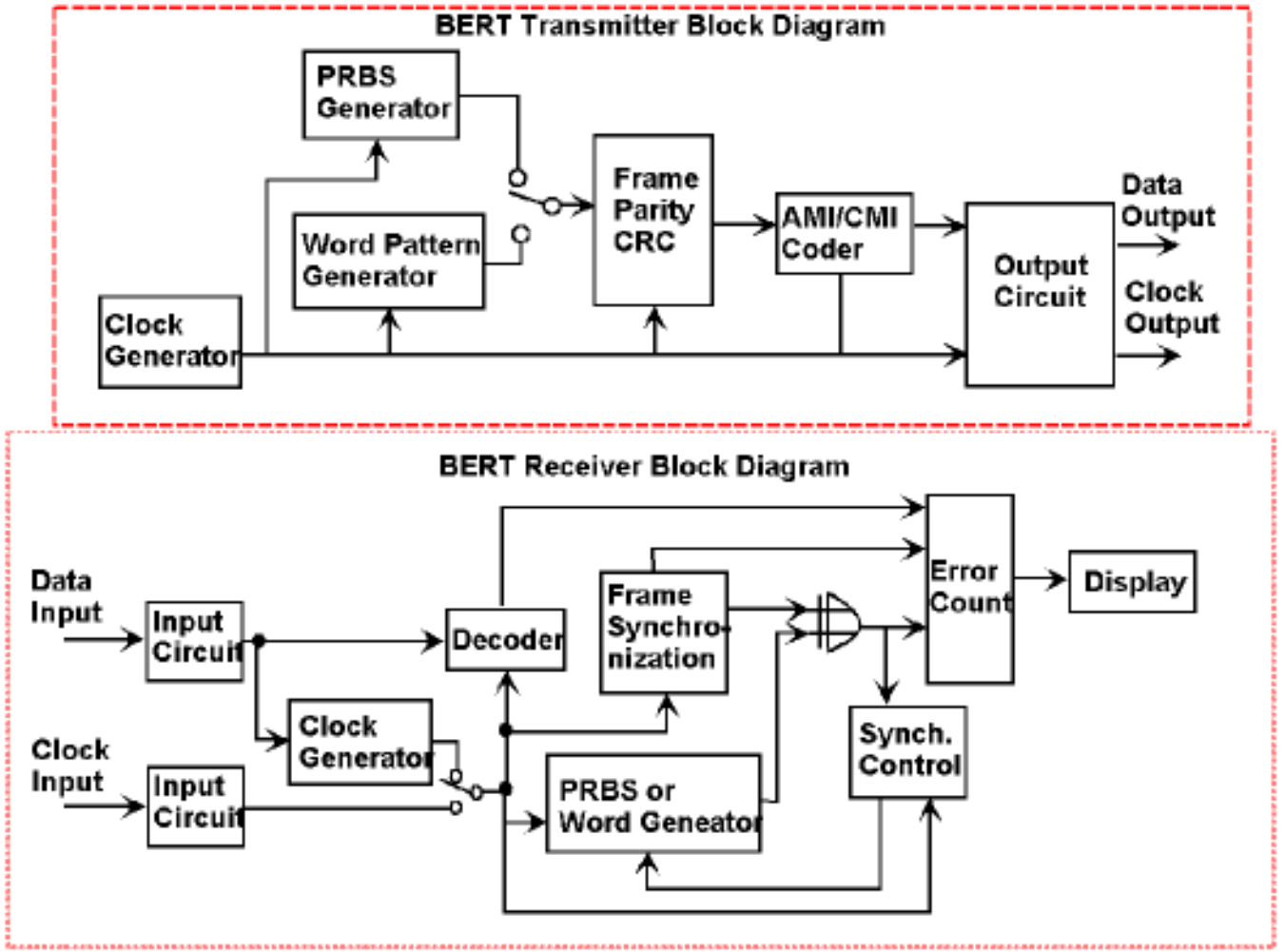
○ =represents data for a given trigger event

*Adapted from "A simple analysis helps to clarify a DSO's performance specs", EDN, Feb. 16, 1989

DSO's (Advantages/Disadvantages)

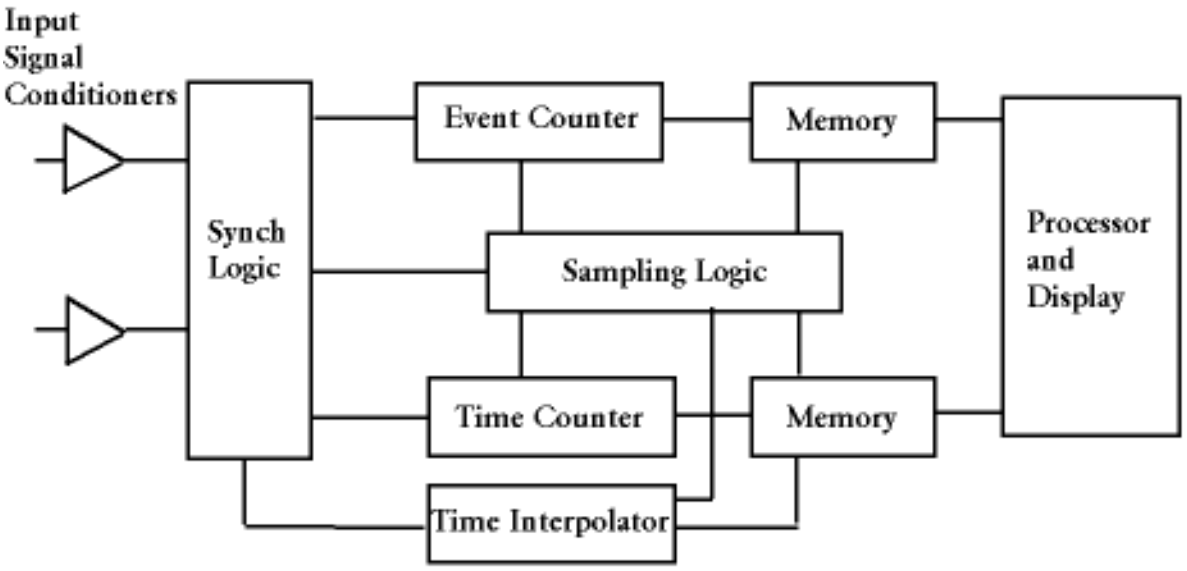
	Real Time Sampling	Random Repetitive Sampling	Sequential Repetitive Sampling
ADVANTAGES	One shot digitizing	Higher BW	Highest BW
		Cheaper A/D required	Cheaper A/D required
		Waveform viewing before trigger	
DISADVANTAGES	Lower BW	Trigger jitter concerns	Trigger jitter concerns
	BW is function of sampling rate BW = Fs/N (N from 2-4)	Require Sample and Hold circuit	Require Sample and Hold circuit
	Require reconstruction (digital filtering)	Not capable of single shot digitizing	Not capable of single shot digitizing
	May require BW limiting (Nyquist Criteria)		Cannot display trigger event without delay line

BERT Block Diagram*



*Adapted from "Basic Knowledge about Error Rate Measuring Instrument" Anritsu, 1992 Technical Note

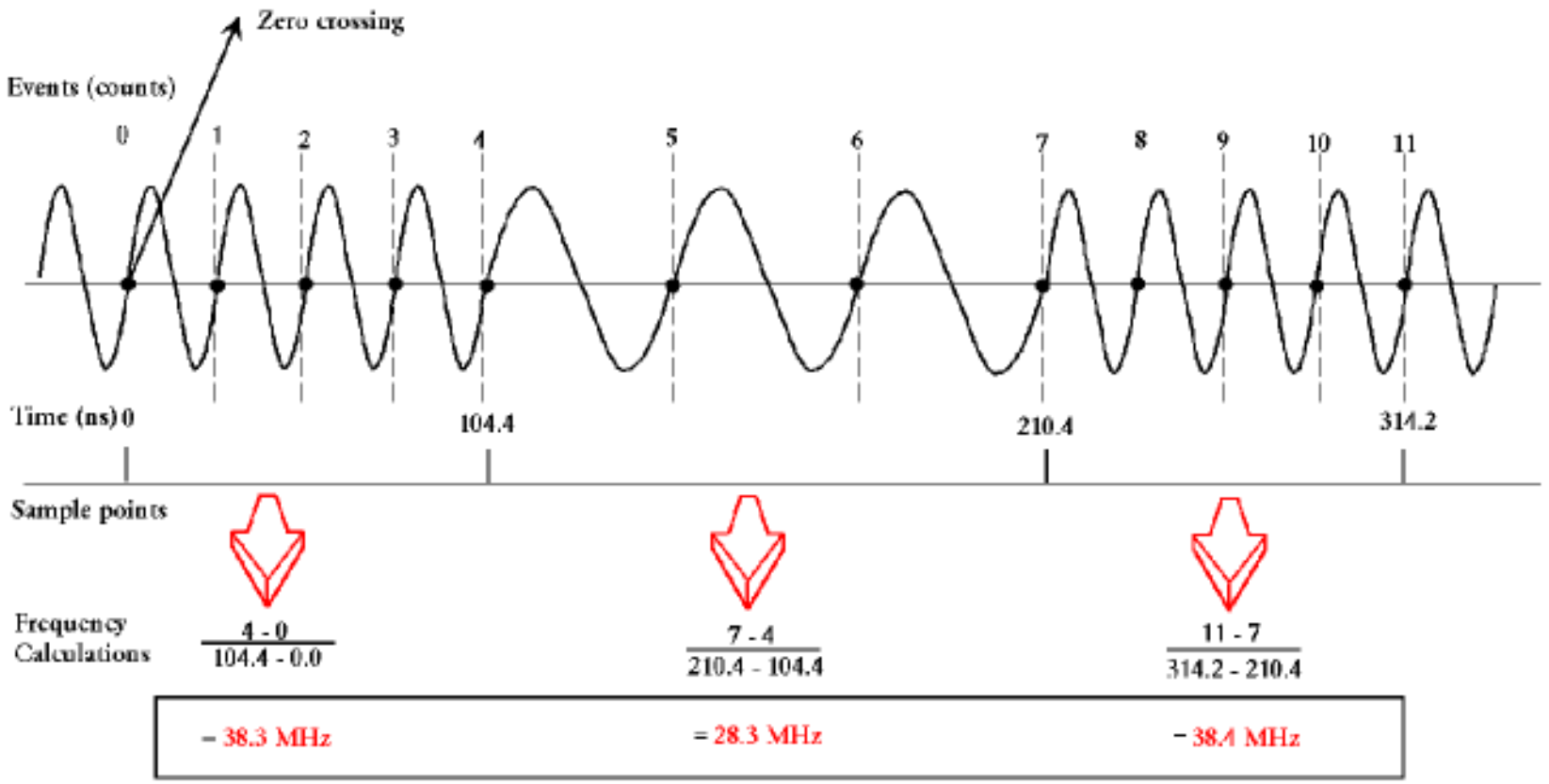
General TIA/MDA Block Diagram*



When sampling logic triggers a sample, the contents of the counters and interpolator is read into the next free memory location. The interpolator is then reset for the next sample point. Samples are taken until the specified number is reached and the memory is then read by the processor for calculations and display. Unlike a counter, the display is often graphic-based.

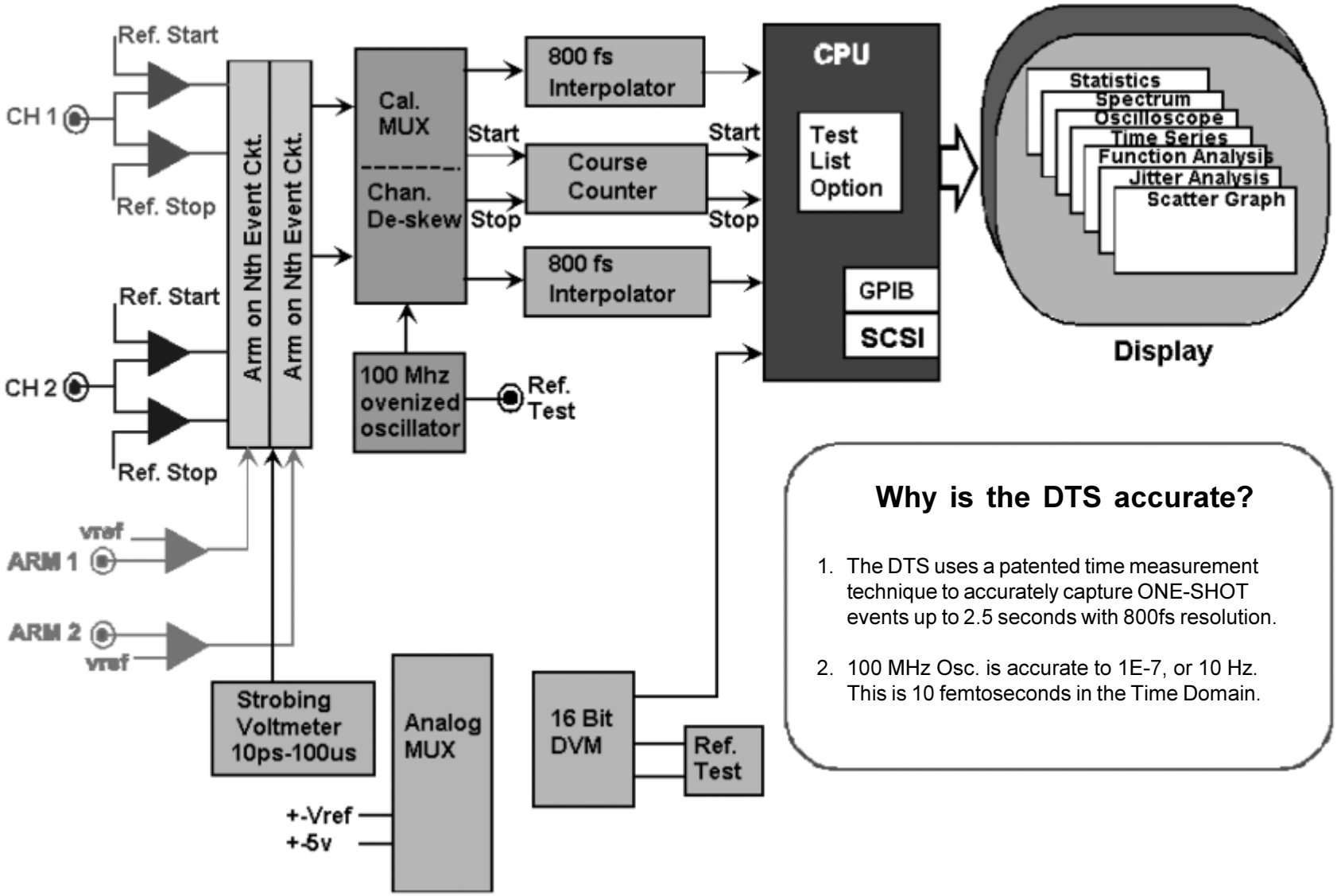
*Adapted from "Basic Instrument Handbook", Coombs, 1996, McGraw-Hill

Basic measurements made by a Time Interval Analyzer/Modulation Domain Analyzer*



*Adapted from "Basic Instrument Handbook", Coombs, 1996, McGraw-Hill

DTS 2070/2075 Block Diagram

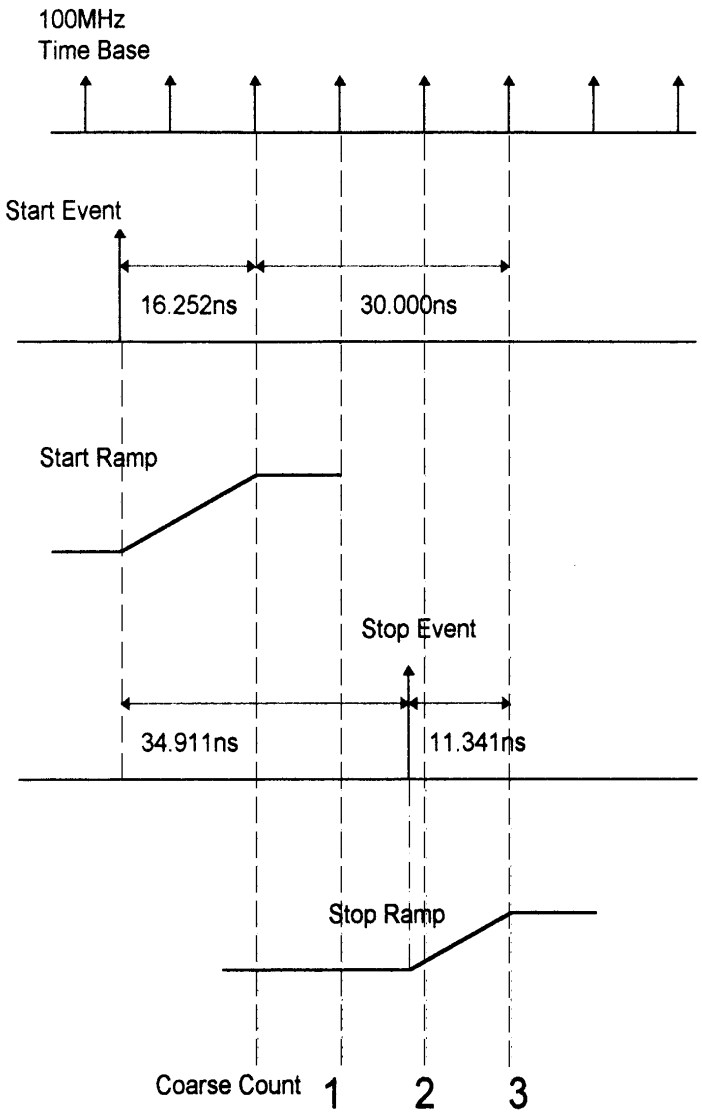


Why is the DTS accurate?

1. The DTS uses a patented time measurement technique to accurately capture ONE-SHOT events up to 2.5 seconds with 800fs resolution.

2. 100 MHz Osc. is accurate to 1E-7, or 10 Hz. This is 10 femtoseconds in the Time Domain.

DTS Time Interval Measurement Technique



Start Ramp Begins at Start Event and Ends at Second Time Base Edge After Start Event.

Stop Ramp Begins at Stop Event and Ends at Second Time Base Edge After Stop Event.

Height of Each Ramp is Digitized using a 14 Bit ADC

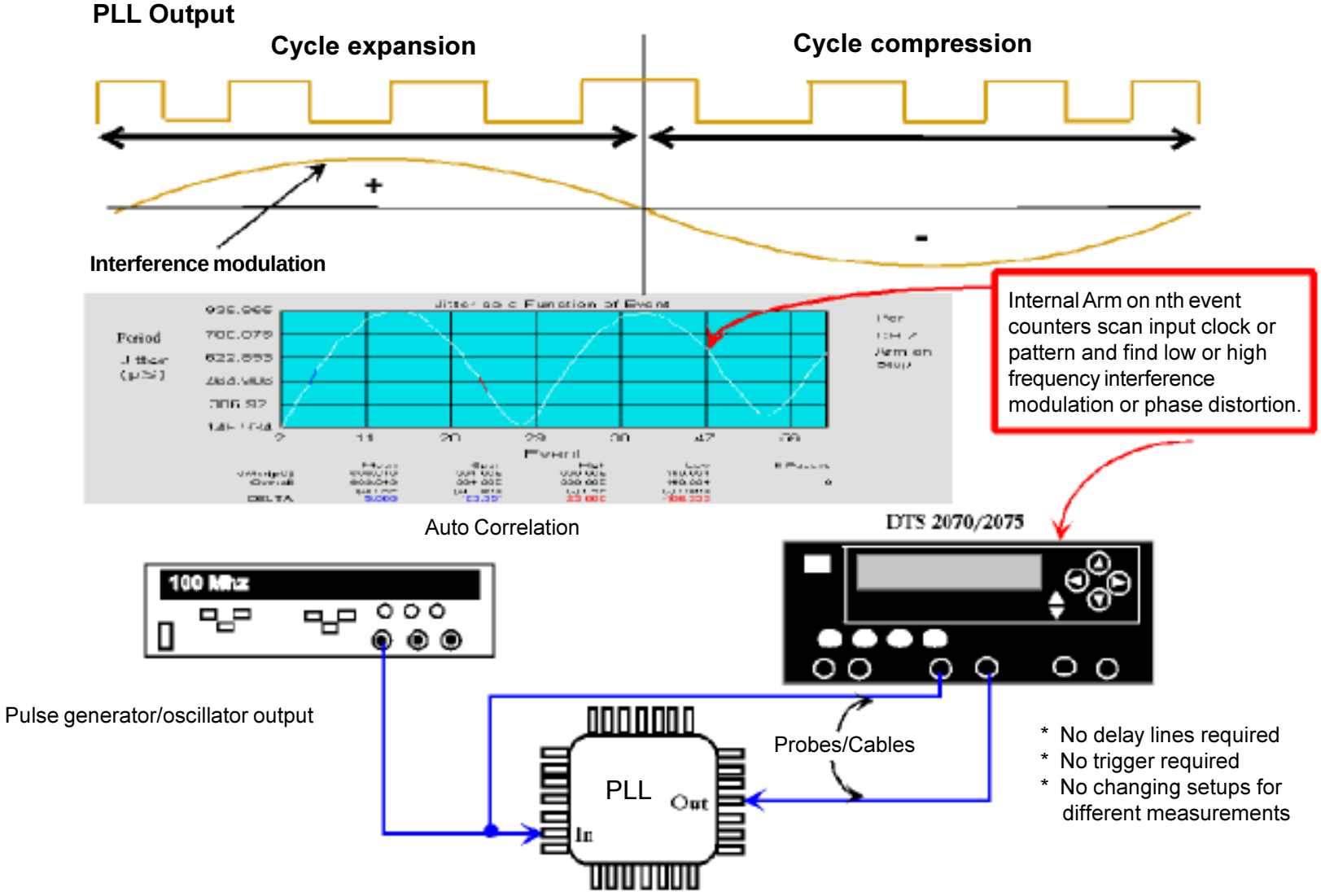
Coarse Counter Counts the Number of Time Base Periods Between Ends of Start and Stop Ramps.

$$N_{coarse\_count} * 10ns + T_{start\_ramp} - T_{stop\_ramp} = T_{measured\_interval}$$

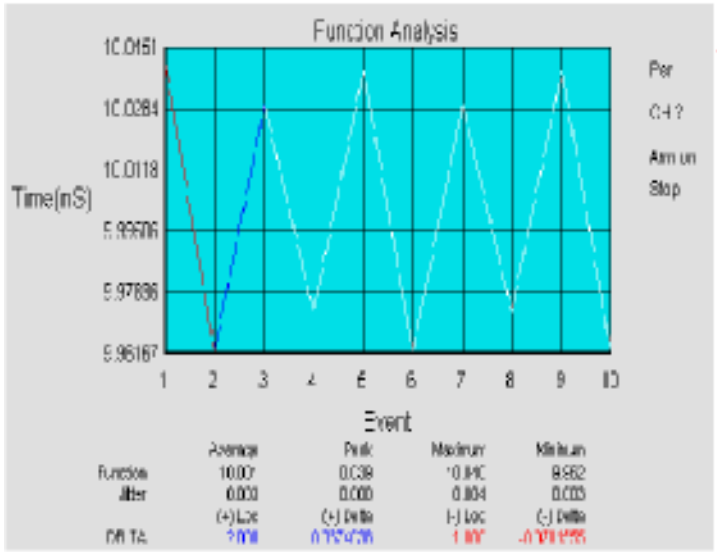
Example:

$$3 * 10.000ns + 16.252ns - 11.341ns = 34.911ns$$

Low Frequency Jitter Analysis (Modulation Domain)



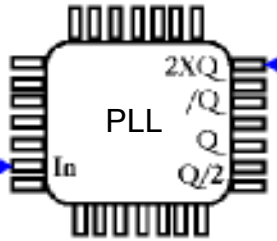
Synchronous Cycle to Cycle Jitter

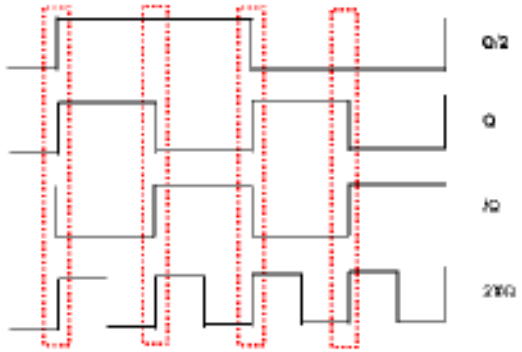


The outputs of the PLL have the following phase relationships. These relationships lead to 4 unique coincidental switching activities. These switching activities lead to 4 repetitive cycle-by-cycle period deviations.

Pulse generator/oscillator

ARM necessary to look at individual pulses in a train





Analysis Tools required to analyze various types of jitter

	Jitter Types				
Jitter Analysis Tools	**Synchronous mod./jitter**	**Asychronous mod./jitter**	**Cycle to cycle jitter (short cycle)**	**I/O Jitter**	**Long Term jitter (Wander)**
Histogram	x	x	x	x	
Freq. based Jitter Analysis (FFT)	x	x	x		
Time based Jitter Analysis (Mod. Domain)	x	x		x	
Function Analysis/Real Time	x		x		
Time Series/Scatter Graph	x	x			x
Waveform Capture	-	-	-	-	-

General Instrument Advantages/Disadvantages

	Jitter Analysis Tools and Features						
Instruments	Histogram	FFT	Jitter Analysis (Time Domain)	Function Analysis (Time/Freq.)	Speed	Waveform Capture	I/O Jitter Capability
DTS 2070/2075	Y	Y	Y	Y	Fast	Y	Y
TIA/MDA*	Y	?	?	?	Fast	N	N
Sampling Scopes*	Y	?	N	N	Slow	Y	Y
Real Time*	Y	?	?	?	Very Slow	Y	N
Digitizers							

*

Key Issues

- instrument noise floor
- f_{max} and bandwidth
- time/voltage resolution
- calibration methodology

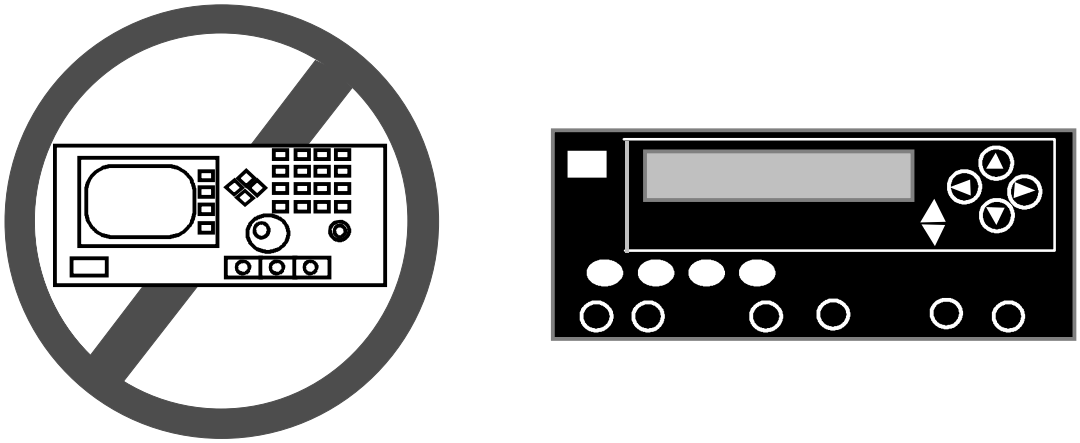
Main Issues for Accurate Jitter Analysis Instrument

- **Maximum usable frequency**
- **Input bandwidth**
- **Jitter noise floor**
- **Smallest one-shot resolution vs. linearity**
- **Correlated measurement record length**
- **Throughput**
- **Frequency/time correlation**

REASONS DTS CAN MEASURE JITTER MODULATION AND DSO CANNOT

CAN I MEASURE JITTER MODULATION??

DSO **DTS 2070/2075**



NO **YES**

- Jitter phase modulation induced onto a clock signal is in the **modulation domain** not the voltage vs. time domain. Modulation domain jitter is at or below the Nyquist frequency of the clock frequency.

- The Digital Sampling Oscilloscope (DSO) with its **trigger** based voltage vs. Time technique does not have the necessary triggering method or record length to capture enough relevant data for adequate determination of jitter in the **modulation domain,** even with using its FFT algorithms.

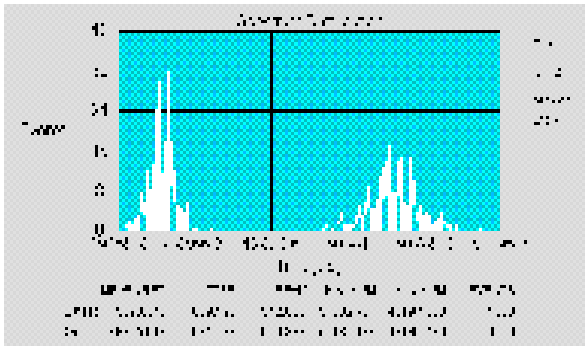
- The DTS 2070/2075 are designed to **directly** measure **modulation domain** information using a hardware and software implementation of a DSP technique called “Auto Correlation”.

UNIQUE PROPERTIES OF DTS 2070/2075

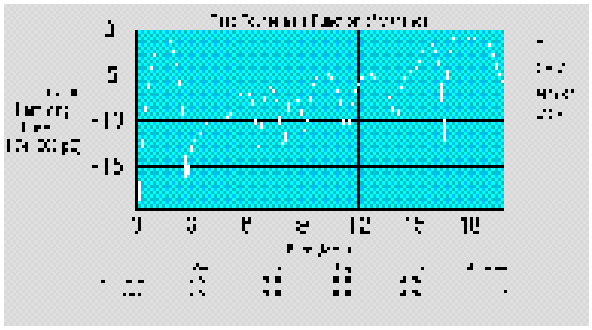
- **42 bits, one range, one-shot time measurement**
- **800fs timing resolution**
- **3ps noise floor**
- **Ability to measure jitter on 10 different pulse timing attributes (TPD++, TPD—, TPD+-, TPD-+, TT+, TT-, PW+, PW-, Period, Frequency); including True I/O jitter measurements.**
- **Arm on nth event (for low frequency modulation and FFT analysis and pattern dependency)**
- **Built in timing and linearity calibration**
- **Two channel De-skewing**
- **DC Calibration of Input Probe effect (if desired)**
- **Measuring events synchronously or asynchronously**
- **Extensive graphical analysis tool**
- **Interface to both popular PC and Unix environment**
- **Easy interface to ATE**

DTS 2070/2075 Measurement Techniques
Examples Of:

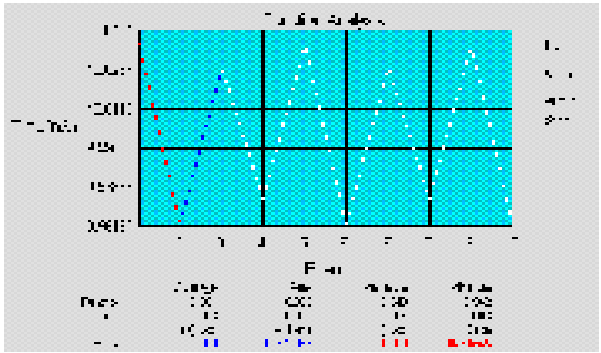
Jitter Histogram
(Threshold Spectrum Analysis)—short cycle



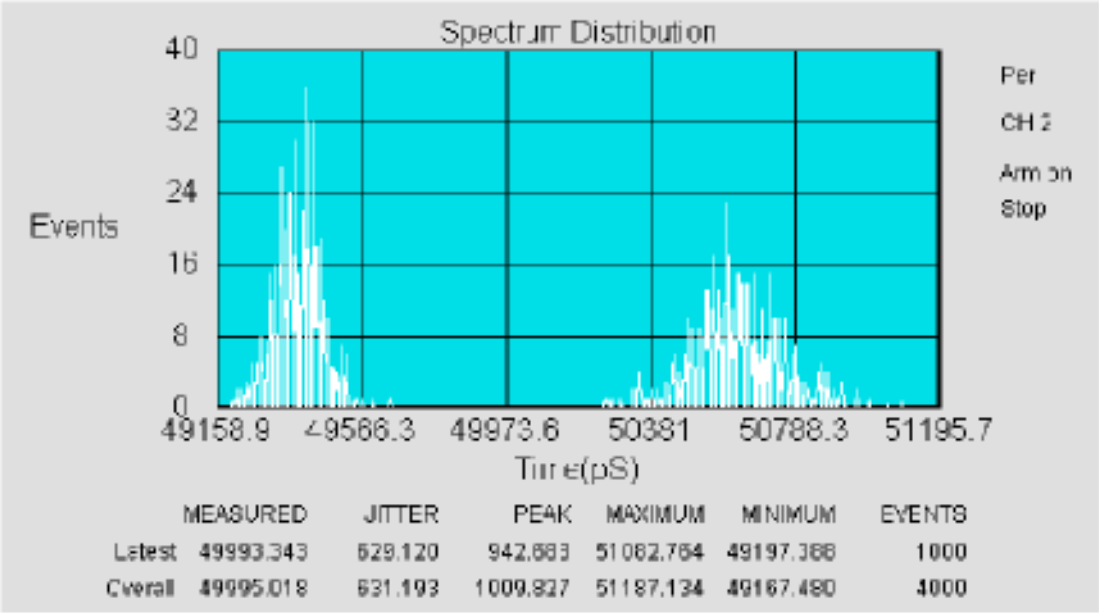
Asynchronous Jitter
(Jitter Analysis)—Modulation Domain



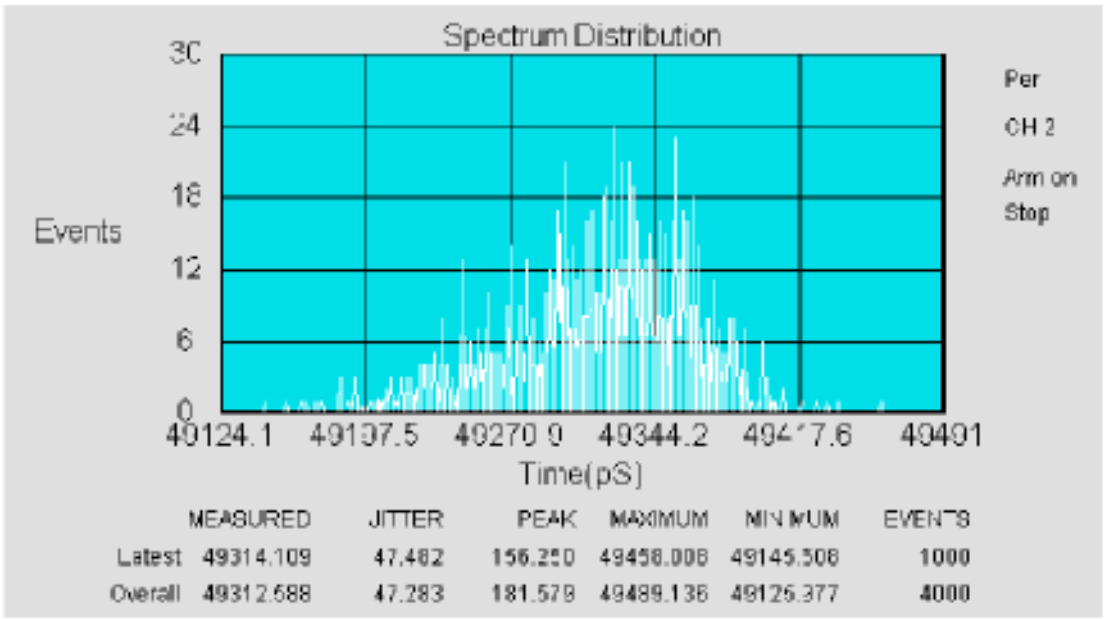
Synchronous Jitter
(Function Analysis)—cycle to cycle



Histogram (Spectrum Analysis)

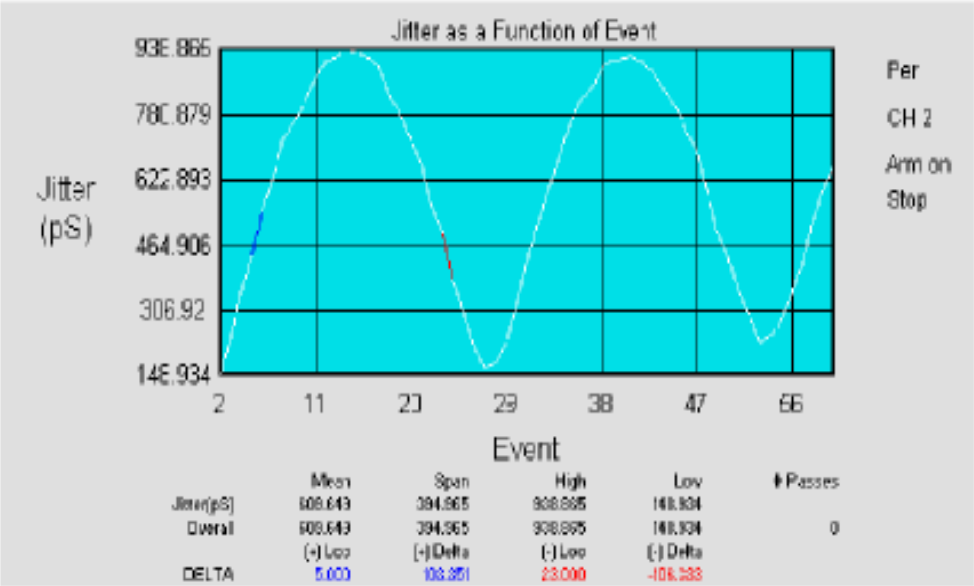


Plot is a period histogram of the 2XQ output of an off the shelf PLL. Input frequency is 10MHz; Output frequency is 20MHz, or 50ns period. Measurement is done automatically without external arming. Sample size = 1000.

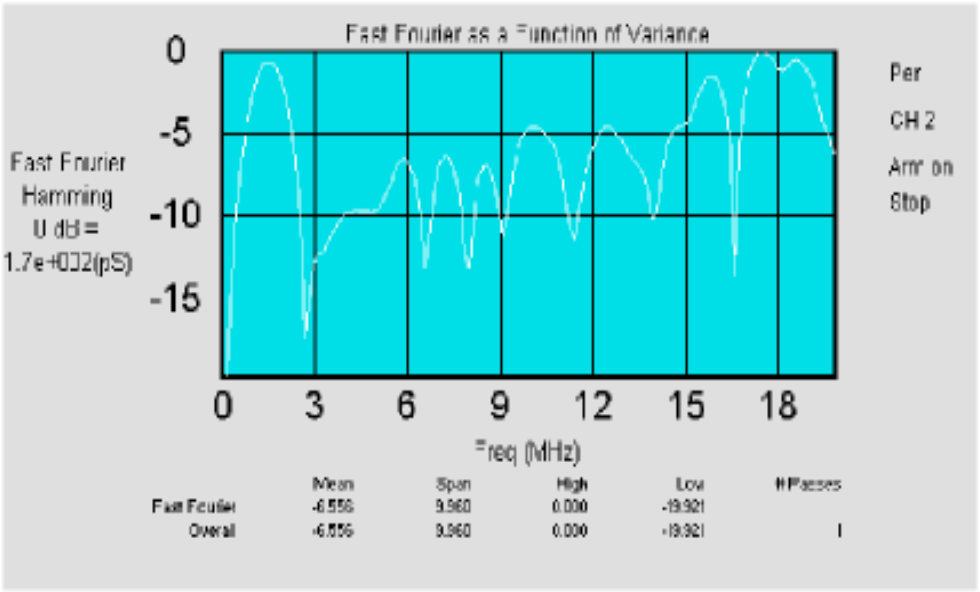


Details are the same as the first plot but external arming was used.

Asynchronous Jitter (Jitter Analysis and FFT)

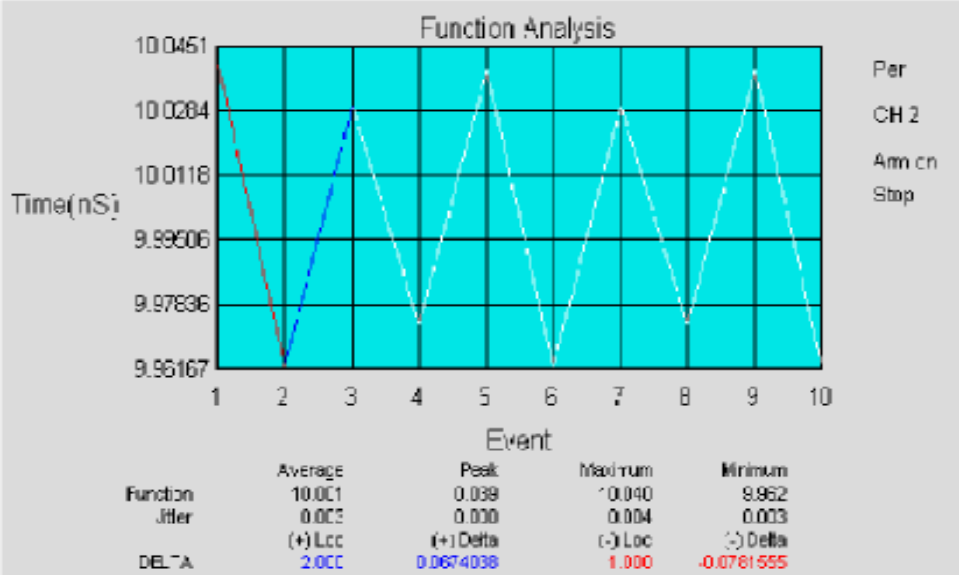


Plot shows jitter accumulation on the 2XQ output of an off-the-shelf PLL. Input frequency equals 20MHz; Output frequency is 40MHz. Plot shows jitter buildup over 28 consecutive cycles.



Plot shows an FFT analysis of the 2XQ output of the PLL with the same conditions used for Jitter Accumulation. Notice the FFT peak at 1.5MHz which corresponds to the modulation frequency calculated in Jitter Analysis (Modulation Domain).

Synchronous Jitter (Function Analysis)



Above is a period Function Analysis plot of the 2XQ output of an off-the-shelf PLL. Input frequency is 50MHz; output is 100MHz or 10ns period.

As can be seen, the period deviation pattern repeats every 4 cycles.

APPENDIX B

CORRELATION ISSUES AMONG INSTRUMENTS

Issues applicable to all instruments*

- Probing
- Fixturing

***Major area leading to correlation issues. In this seminar, an assumption is made that participants are knowledgable in these two areas and are using best lab practices.**

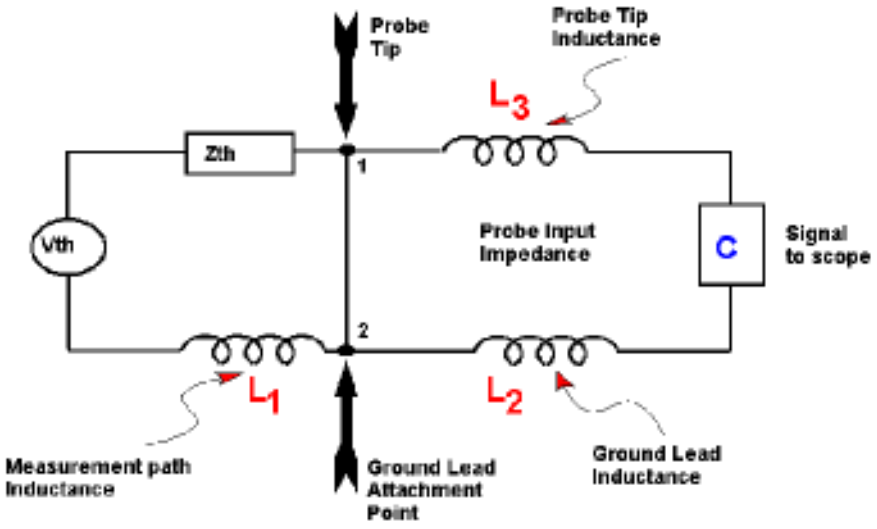
Issues dependent on particular instruments

- Equipment resolution/accuracy vs. range and other specifications
- Instrument noise floor
- Record Length (ability to resolve low frequency modulation)
- Asynchronous vs. Synchronous measurements
- Instrument Calibration techniques
- Operating beyond equipment limitations
- Instrument Setting
- Changes in external environment (temp./Vcc noise/line noise, etc.)

IDEAL PROBE

- Infinite Bandwidth
- Zero input capacitance
- Infinite input resistance
- Infinite dynamic range
- Attenuation of 1
- Zero delay
- Zero phase shift
- Mechanically well suited to application

Ground Lead Resonance*



$$F = \frac{1}{2\pi\sqrt{LC}}$$

$$T_R = \frac{.35}{BW}$$

F = Resonance Frequency

T_R = 10%-90% Rise Time

$L = L_1 + L_2 + L_3$

BW = Probe Bandwdith

C = Probe Tip Capacitance

Example:

L = 100 nH (4 inches of ground lead @25 nH/in.)

C = 8 pF

$$F = \frac{1}{6.28\sqrt{(100\times10^{9})(8\times10^{-12})}}$$

$$T_R = \frac{.35}{178\ MHz}$$

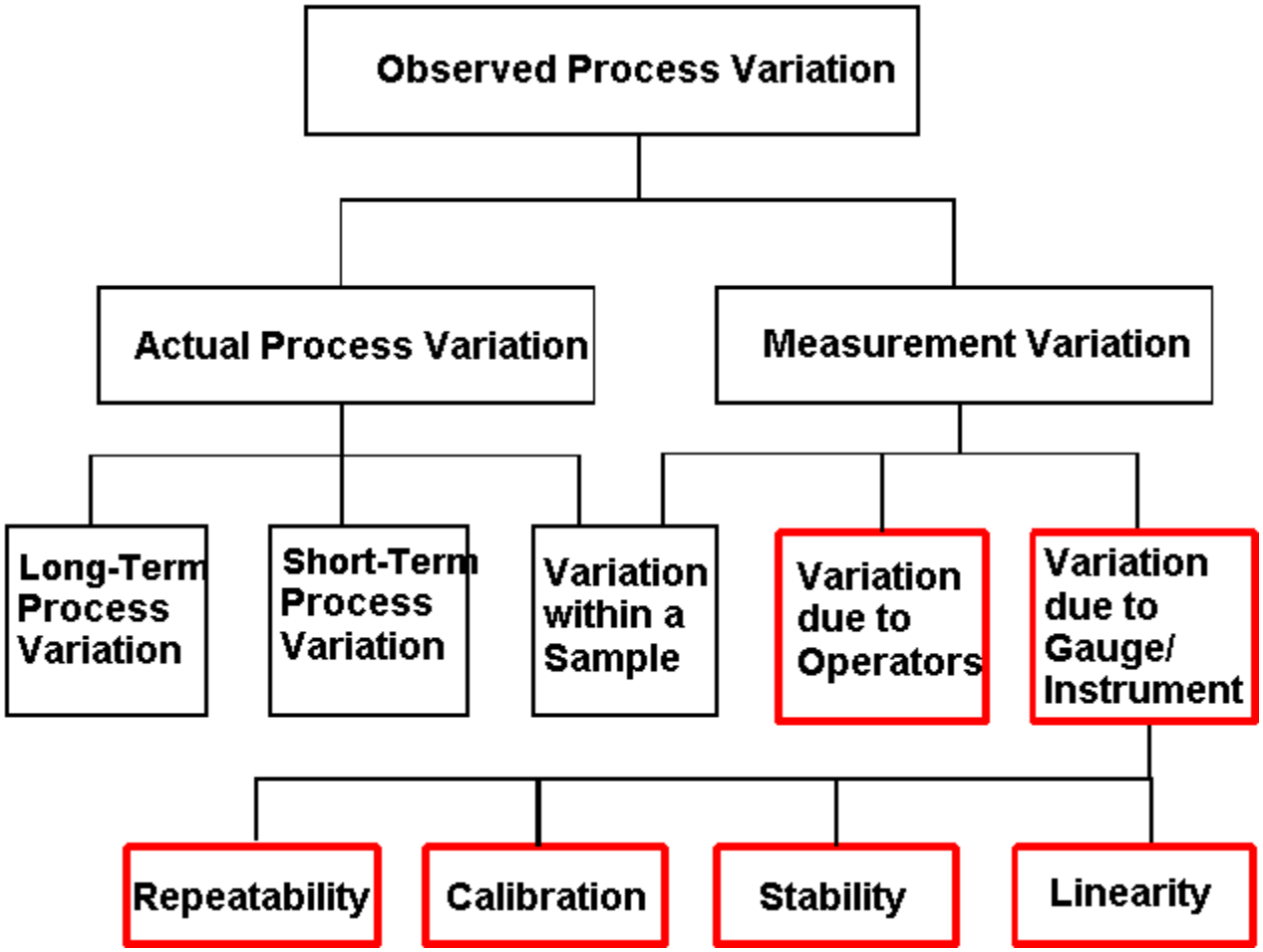
F = 178 MHz

T_R = 1.9 ns

Therefore a signal with a harmonic component of 178 MHz will ring.

*Adapted from "How an oscilloscope works", HP scope manual

Repeatability and Reproducibility*



- Repeatability (Is there variation of the gauge when used by one operator in a brief time interval?)
- Calibration (Is the gauge accurate?)
- Stability (Does the gauge change over time?)
- Linearity (Is the gauge more accurate at low values than at high values?)

☐=areas uniquely addressed by the DTS instrument

*adapted from Concepts for R&R Studies

Correlation issue examples

With DSO

(will show issues with delay setting and using hardware vs. software measure)

(will show jitter dependency on trigger source)

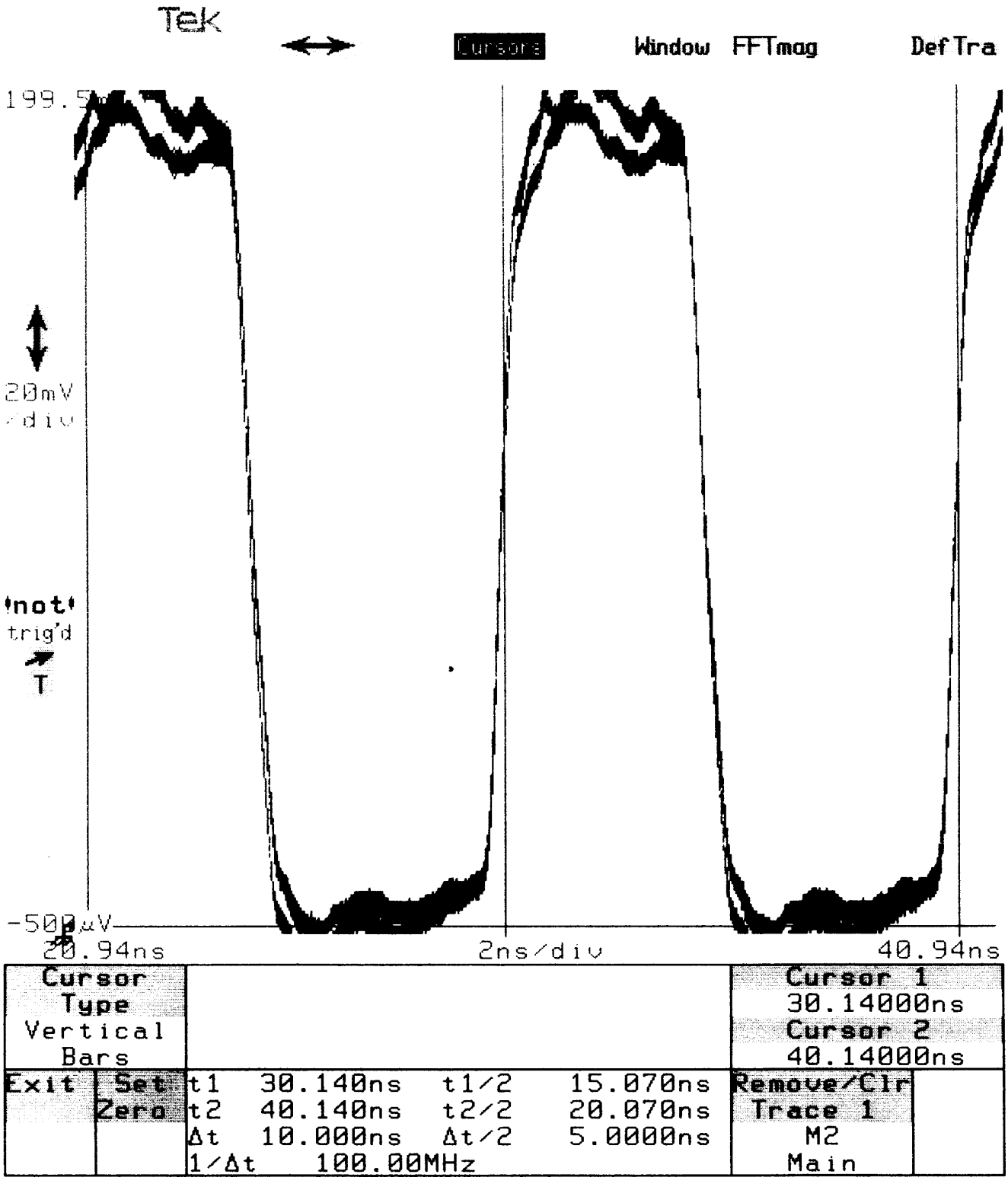
With Real Time Digitizer

(will show resolution issues and record length issues)

With TIA

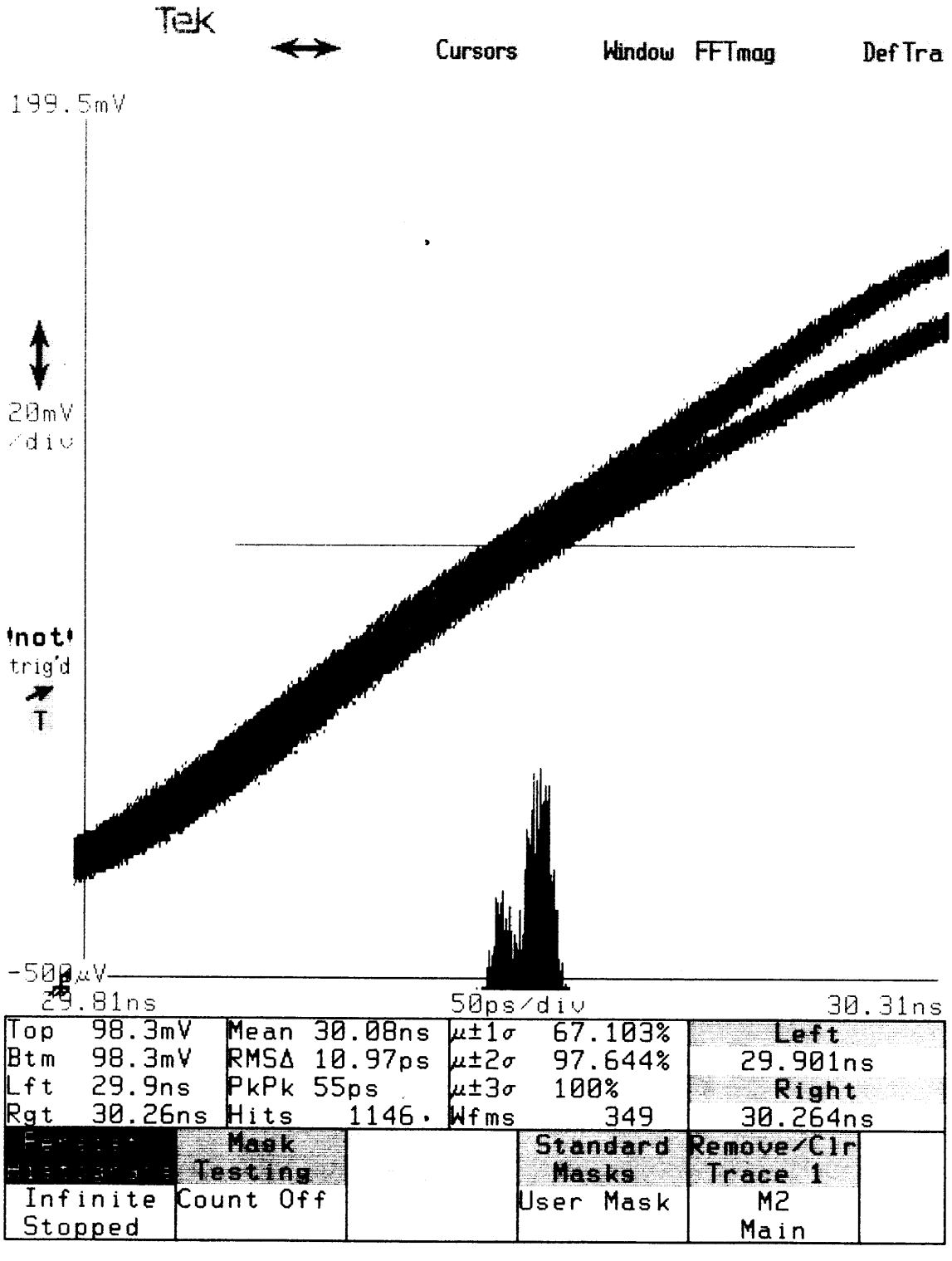
(will highlight limitations from supplier data sheet for product)

CSA803A COMMUNICATIONS SIGNAL ANALYZER
date: 24-APR-97 time: 18:13:01



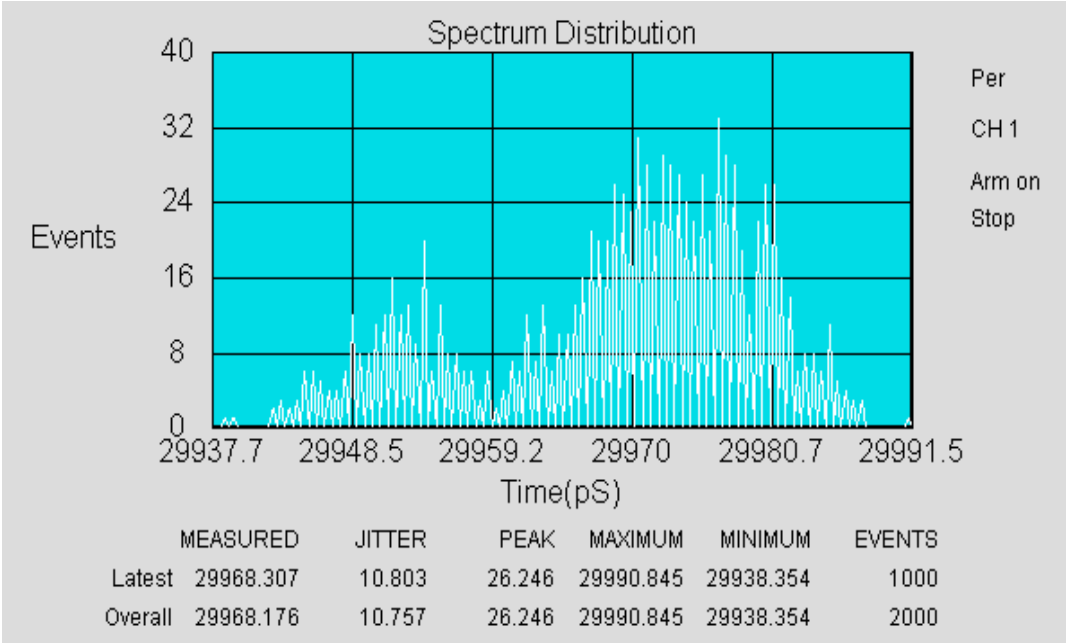
– 100MHZ PLL output triggered by signal via splitter

CSA803A COMMUNICATIONS SIGNAL ANALYZER
date: 24-APR-97 time: 18:02:28



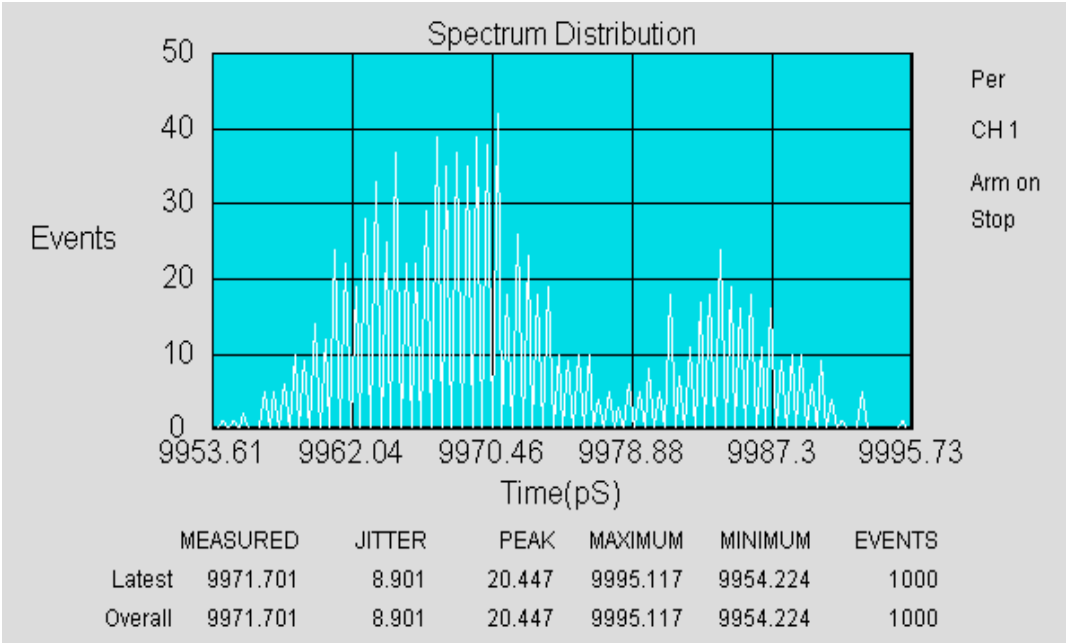
– 100MHZ PLL output triggered by signal
– Looking at 3rd cycle which is first measurable cycle

DTS FIRST PERIOD JITTER MEASUREMENT



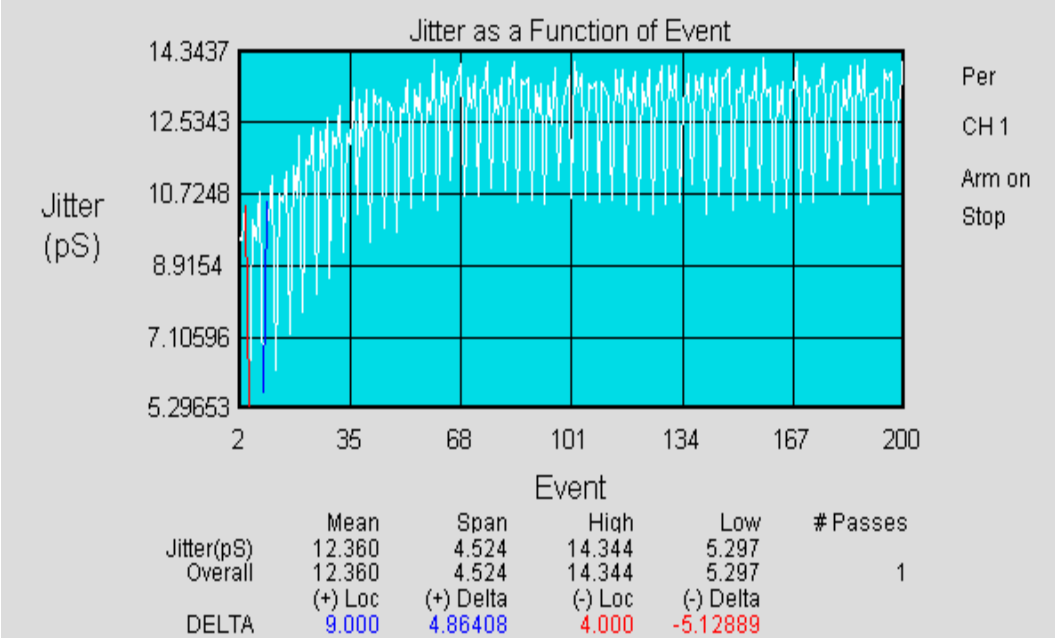
	MEASURED	JITTER	PEAK	MAXIMUM	MINIMUM	EVENTS
Latest	29968.307	10.803	26.246	29990.845	29938.354	1000
Overall	29968.176	10.757	26.246	29990.845	29938.354	2000

100 MHz (10ns) PLL output. For comparing to CSA 803A, DTS measures time duration from rising edge 1 to rising edge 4 or effectively 3 cycles. As can be seen, the DTS correlates well in rms jitter and shape of the bimodal histograms.

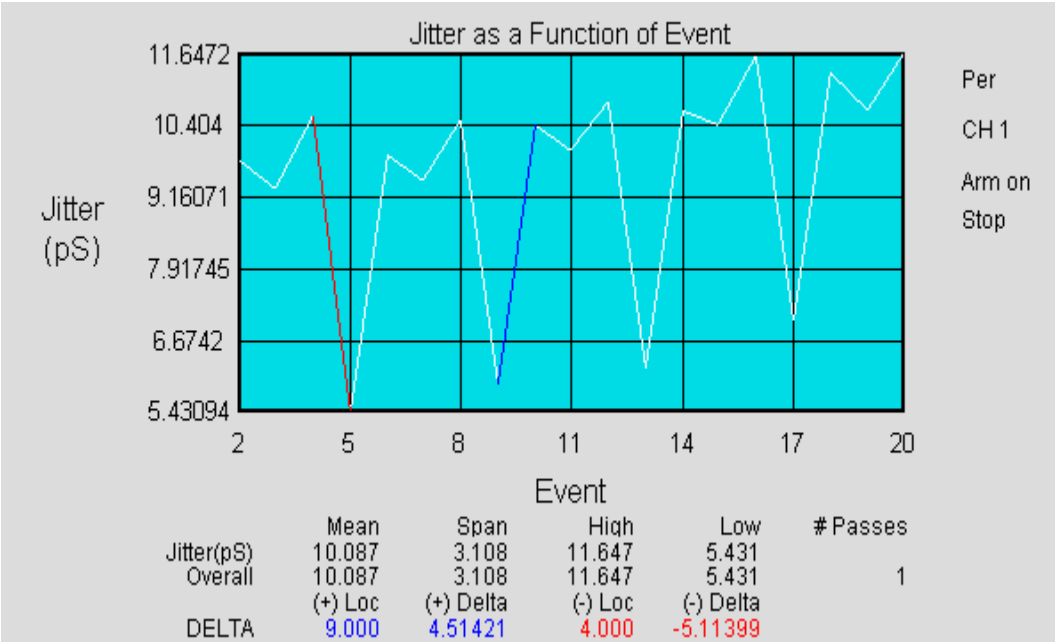


	MEASURED	JITTER	PEAK	MAXIMUM	MINIMUM	EVENTS
Latest	9971.701	8.901	20.447	9995.117	9954.224	1000
Overall	9971.701	8.901	20.447	9995.117	9954.224	1000

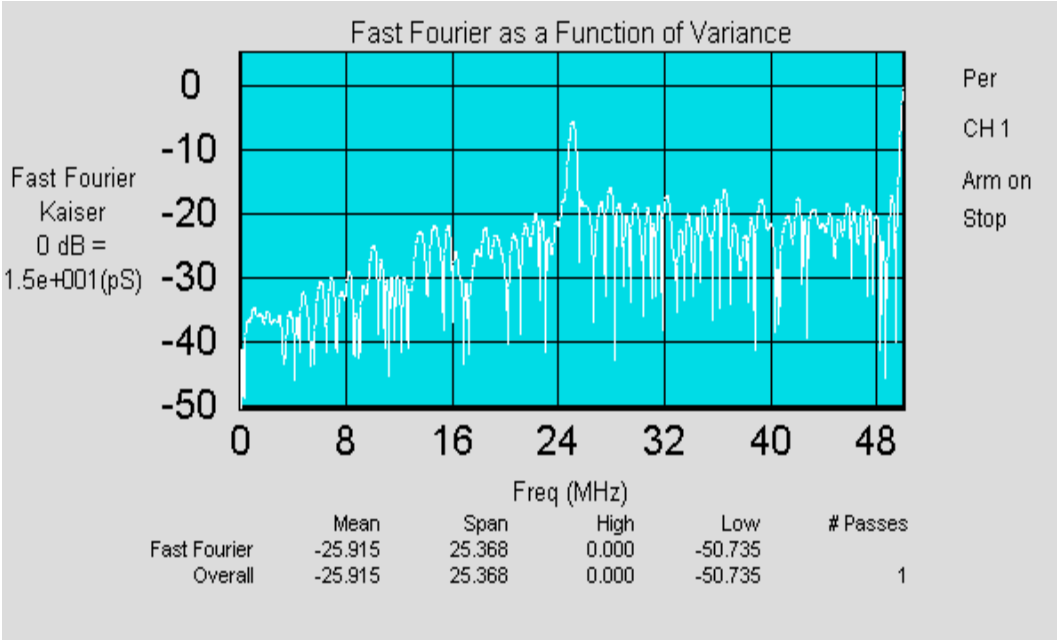
Same signal as above, except DTS is measuring from 1 rising edge to 2nd rising edge (1 cycle or period). Notice lower jitter and shifting of histogram shapes. CSA 803A cannot easily measure just 1 cycle because of minimum delay requirement.



Jitter Analysis of 100 MHz PLL output. Up to count 200. Notice the accumulated jitter modulation in the time domain.

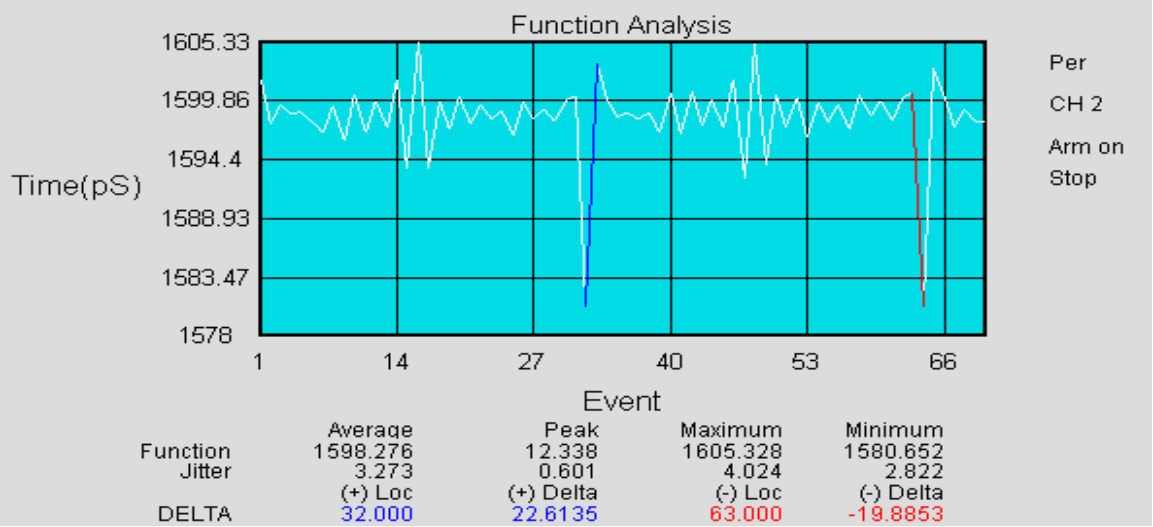


Jitter Analysis of 100 MHz PLL output. Count was set to 20. This is a zoomed plot of the above. Notice the distinct pattern to the accumulated jitter.

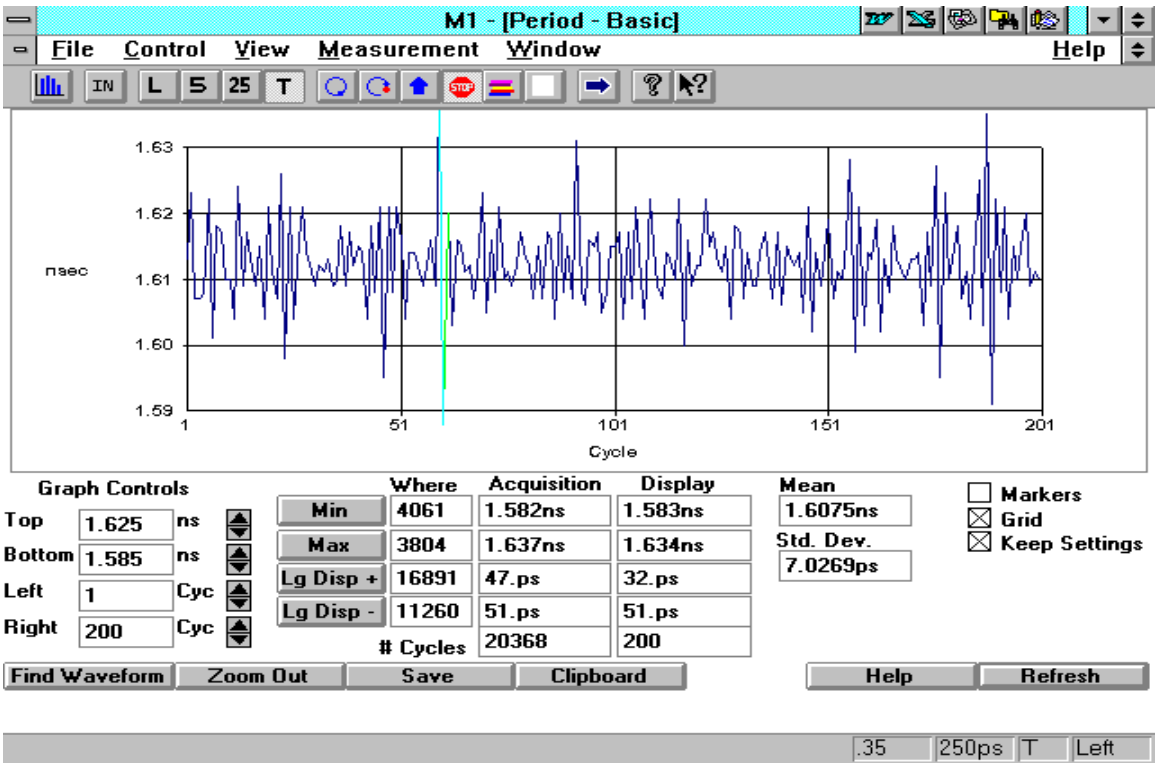


Jitter Analysis FFT of 100MHz PLL output. Modulation detected at 50 and 25 MHz.

Real Time Digitizer Correlation issue (resolution)

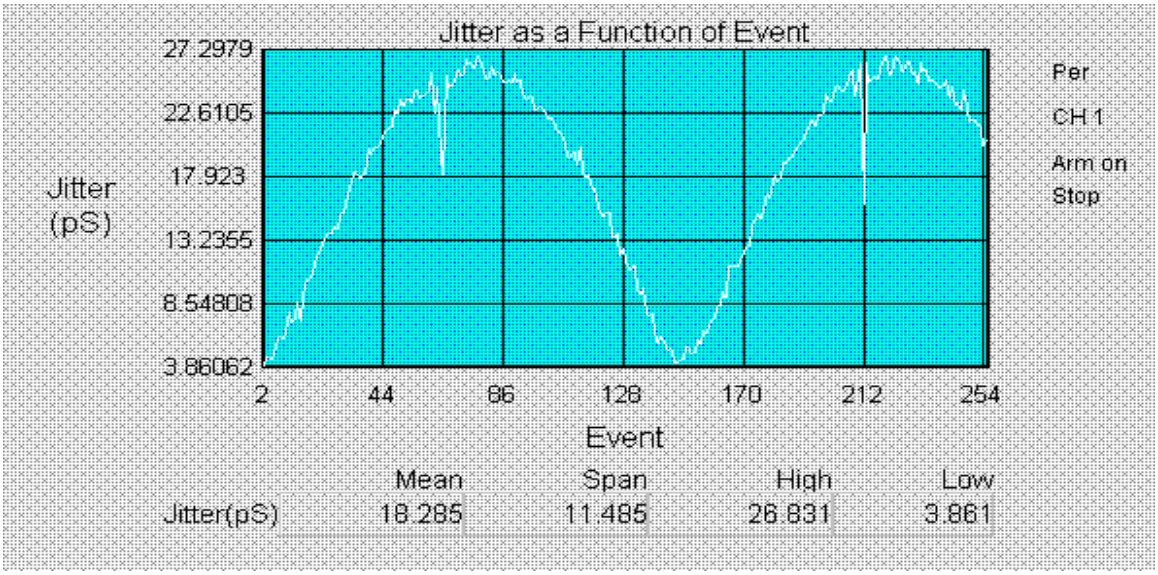


Above is a DTS 2070 Function Analysis plot on a 622 MHz ATM device. Notice the 20 ps short cycle every 32 cycles. The 800 fs resolution of DTS 2070 allows one to "see" the small period push out.

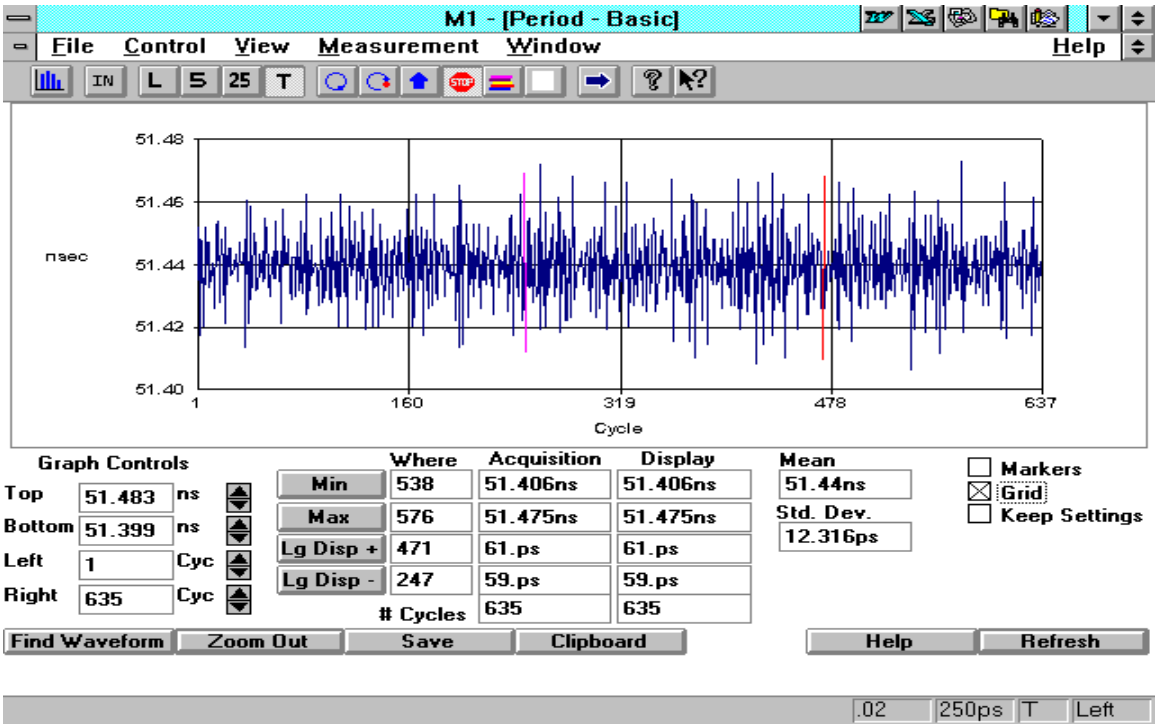


The above is a cycle by cycle plot using a 4 GSa/sec real time digitizer with custom software. You cannot resolve the 20 ps period push out due to the lower resolution of the digitizer.

Real Time Digitizer Correlation issue (small record length)



Above is DTS 2070 Jitter Analysis plot for a 19.4 MHz oscillator signal to an ATM device. This modulation is caused by the 130 kHz switching power supply coupling to the test fixture.



The above plot is a cycle by cycle plot using a 4 GSa/sec real time digitizer with custom post processing software. You cannot see any modulation due to the small record length.

TIA/MDA Performance Limitations

5372A*

Frequency range 16 kHz to 13 MHz
Singe Shot Resolution 150ps
Single Shot Accuracy ..... +-250ps
RMS Jitter noise floor ..... <=160ps
Input Bandwidth 500 MHz

Using FFT option ($3000 additional cost)

The FFT is not supported for the following measurement functions:

- Rise Time
- Fall Time
- Positive Pulse Width
- Negative Pulse Width
- Duty Cycle
- Peak Amplitude
- Histogram Time Interval
- Histogram Continuous Time Interval
- Histogram+- Time Interval

HP E1725A*

Sample Rate

The maximum frequency that can be time stamped any time is 80 MHz. However, this parameter controls the maximum rate at which every edge can be captured. For single channel measurements, every edge of a clock can be captured up to the indicated Sample Rate (e.g. to 80 MHz with the Sample Rate set to 80 MHz). However, there are trade-offs with the Sample Rate setting as summarized in this table.

Sample Rate	Pacing	Min. Freq.	Max. Time Interval
80 MHz	Auto	4 MHz	250 ns
	Manual	625 kHz	1.7 us

If the signal frequency goes below the minimum frequency, it will be measured incorrectly or not at all. If any time interval between clock edges is longer than the maximum time interval (actually the maximum time between time stamps), it will be measured incorrectly or not at all. Note that the limits change with the setting of the Pace parameter.

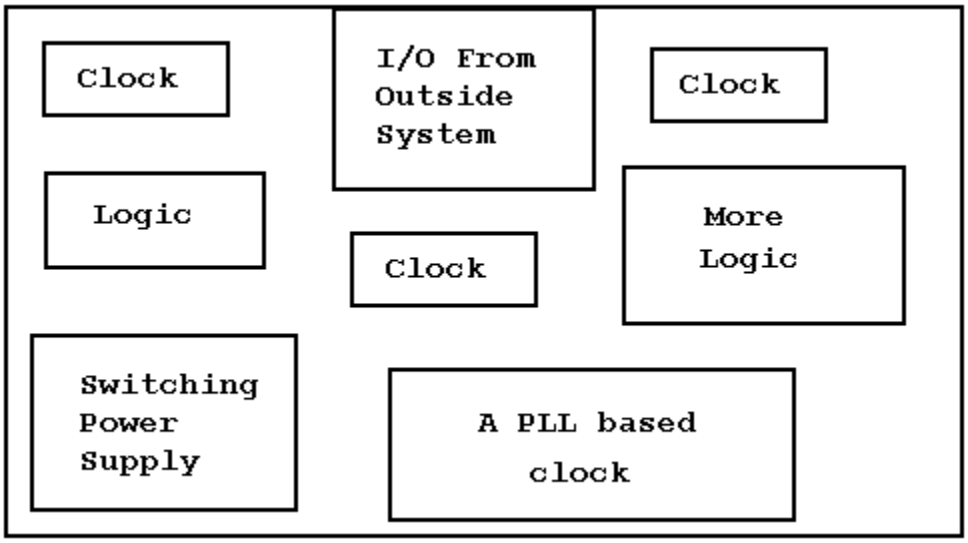
*Information from HP literature

APPENDIX C
FFT-Based Jitter Analysis

- Sources of periodic jitter
- A display of jitter
- Basic measurement and random measurements
- Effective sampling rate
- Variance of measurements
- Aliasing
- DSP procedure with graphs
- FFT graphs showing
  -how padding improves graph
  -behavior of various windows
  -aliasing
  -low frequency jitter analysis

Sources of Periodic Jitter:

A Digital System;



Some causes of periodic jitter:

-crosstalk between clocks

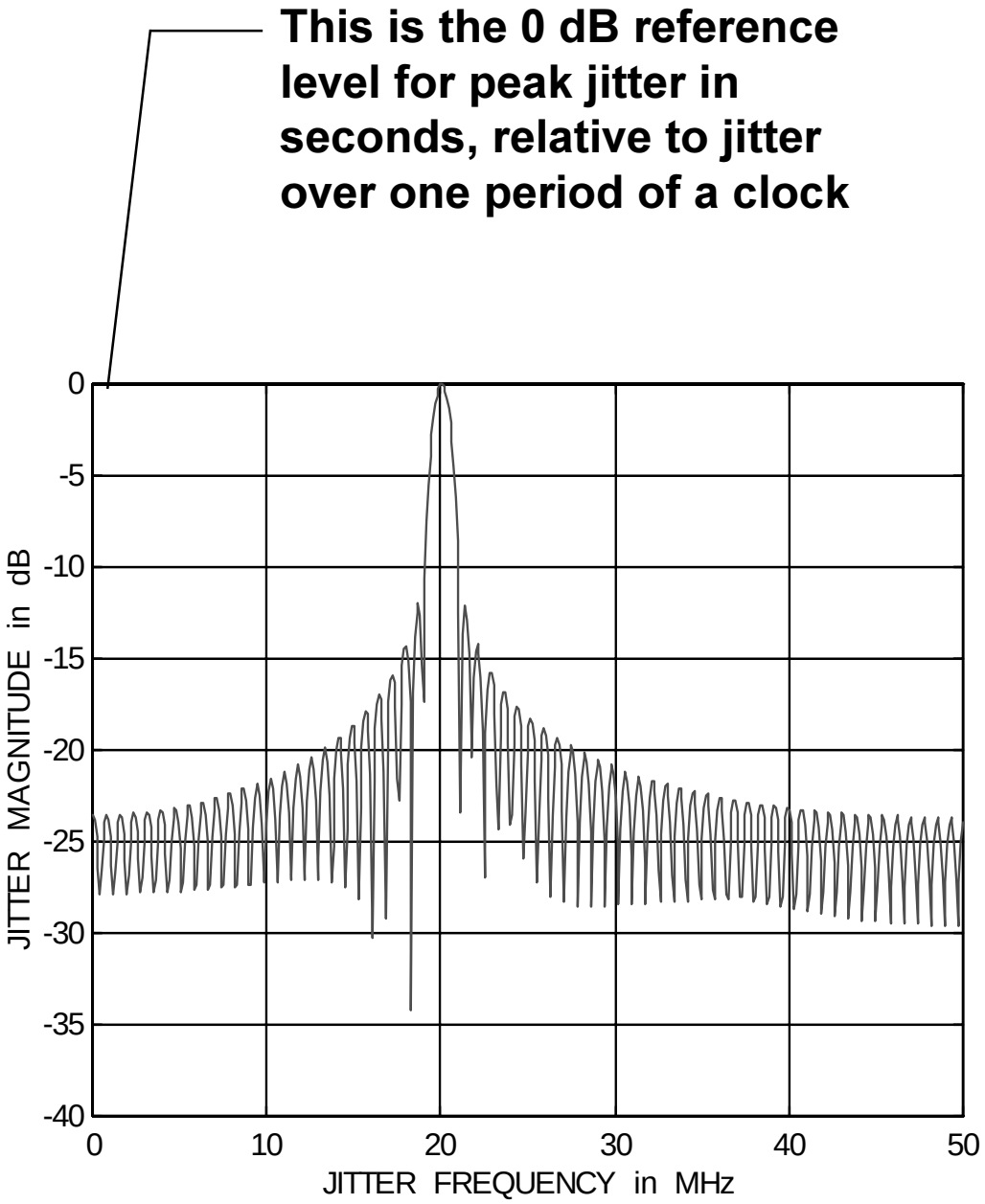
-SPS ripple - Frequency modulates a PLL

-crosstalk between a clock and a counter, which is driven by the same clock

-EMI coming in through I/O cables; a nearby radio station

A Frequency Domain Analysis Tool helps to diagnose a Digital System which has problems with Periodic Jitter.

Jitter Spectrum

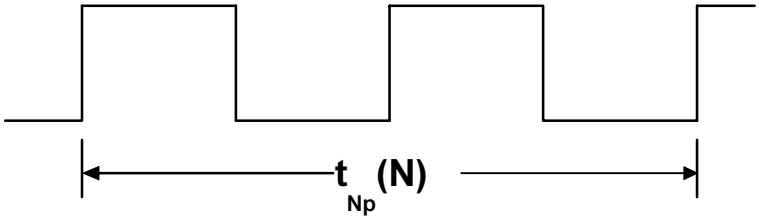


-Actual display will print the 0 dB reference level in seconds peak

Basic measurement and random measurements:

The basic measurement, $t_{Np}(N)$:

A Clock:

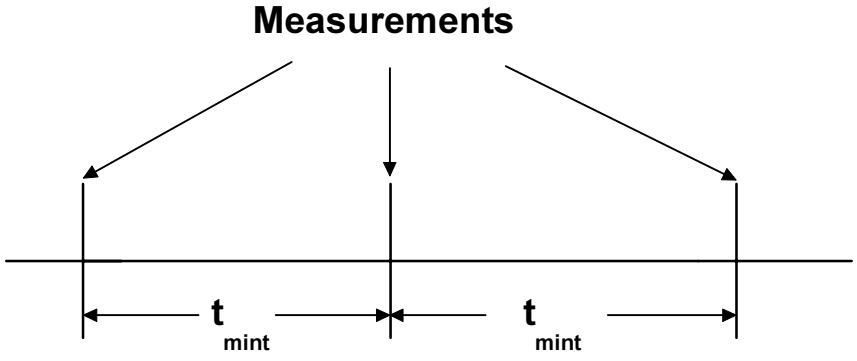


$t_{Np}(N)$ is the measured time interval of N periods of a clock

In this case N = 2

This is a real time measurement

Random measurements:



t_{mint} varies from 21us to 25us

t_{mint} is the measurement interval

Effective sampling rate:

Measurement schedule for $t_{Np}(N)$;

$N = \{1,1*N_{step}+1,2*N_{step}+1,...,N_{max}\}$

N_{step} is the step size of N
N_{max} is the maximum value of N

Effective sampling rate; $f_s = \bar{f}_{clock}/N_{step}$

$\bar{f}_{clock}$ is the mean clock frequency

Variance of $t_{Np}(N)$:

$$VARIANCE[t_{Np}(N)] = (1/M_{meas}) \sum_{j=1}^{M_{meas}} [t_{Np}(N)-\bar{t}_{Np}(N)]^2$$

$\bar{t}_{Np}(N)$ is the mean value of $t_{Np}(N)$, for a given N

M_{meas} is the number of measurements taken for each N
M_{meas} is usually set from 100 to 10,000

$N = \{1,1*N_{step}+1,2*N_{step}+1,...,N_{max}\}$

$$\bar{t}_{Np}(N) =(1/M_{meas}) \sum_{j=1}^{M_{meas}} t_{Np}(N)$$

Aliasing:

An alias is that which is not what it seems to be. An alias is a pretender.

If $f_{pj} > f_s/2$, the Nyquist frequency, the measured jitter frequency will be less than $f_s/2$,

$\mathbf{f_{pj}}$ is the periodic jitter frequency

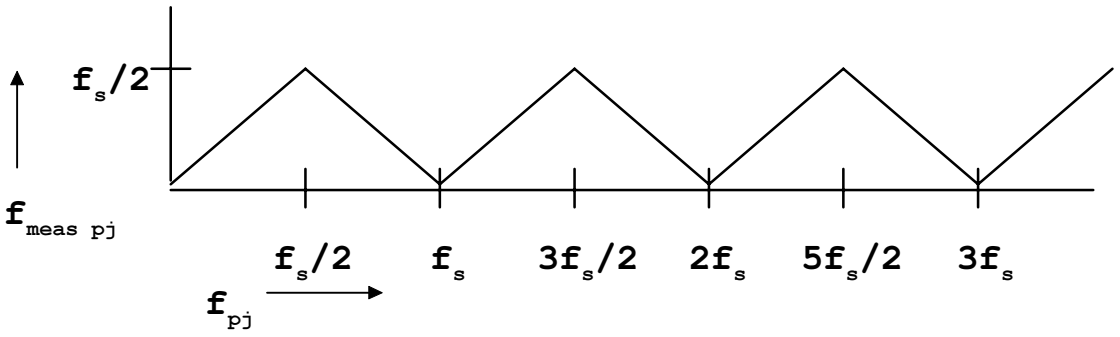
$\mathbf{f_s}$ is the effective sampling rate

$$\mathbf{f_{meas\ pj} = MINIMUM[ABS(k*fs-f_{pj})],}$$

ABS is the absolute value function

$\mathbf{f_{meas\ pj}}$ is the measured periodic jitter frequency

k = {1,2,3...}



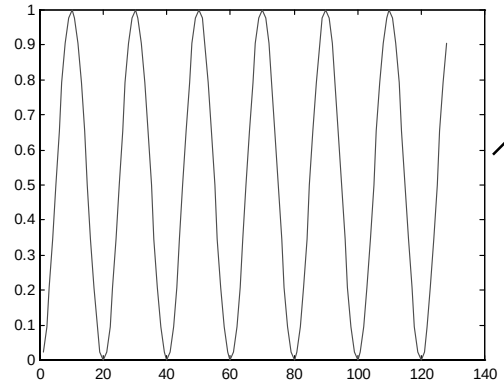
When $f_s=f_{clock}$ ($N_{step}=1$), the alias products are real

Example:

f_s = 100MHz, f_{pj} = 260MHz (4th harmonic of 65MHz)
$f_{meas\ pj}$ = 40MHz, this is less than 50MHz, $f_s/2$

calculation: $f_{meas\ pj}$ = ABS(3*100 MHz-260 MHz)
(k = 3)

Our Procedure to obtain a Frequency Domain display of Periodic Jitter:



TIME in periods of 1/fs

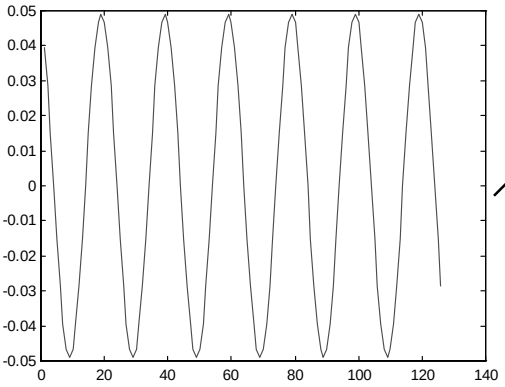
VARIANCE[t_{Np}(N)]

Measurement schedule: Nmax=128
Nstep=1

Jitter source is one sine wave.

Magnitude is in seconds squared or "jitter squared" (power).

This is a display of the auto-correlation function of periodic jitter (one tone).

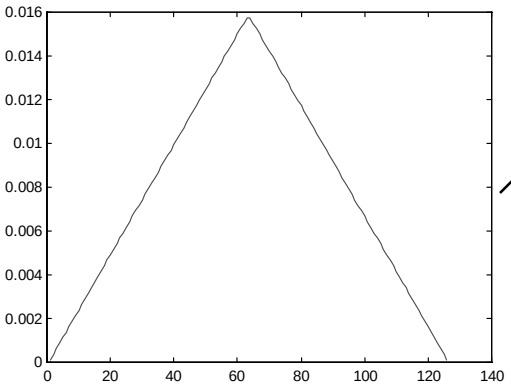


Second derivative of VARIANCE[t_{Np}(N)].

This normalizes the magnitude to jitter over one clock period.

Notice that the second derivative has shifted the phase 180 degrees.

Two data points have been lost by performing this function.

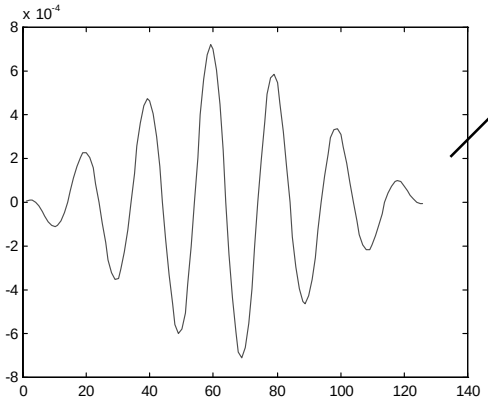


This is a window; in this case a triangular window.

The type of window selected determines the bandwidth and stop-band rejection of each FFT output point (bin).

The second derivative of VARIANCE is multiplied by this window.

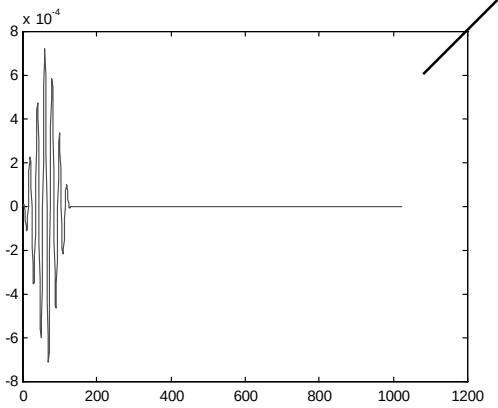
continued to next page



A graph of the window times the second derivative of VARIANCE(N).

Notice that the magnitude of the plot is tapered from the center to the ends.

We are still in the seconds squared domain (jitter power).



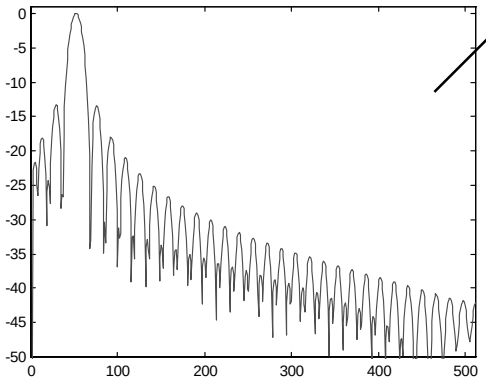
TIME ⟶

The data has been padded with zeros. The padding factor is 8.

898 zeros have been added to the end of the data record and now has a length of 1024, suitable for a Radix 2 FFT input.

Padding increases the frequency resolution of the FFT, resulting in a better looking display and it also has increased amplitude accuracy. It also reduces "picket fencing" error.

A Radix 2 FFT is executed:



FREQUENCY ⟶

The square-root of the FFT output bins is taken; we are now in the jitter domain (not jitter squared).

A $20*\log_{10}$ is performed and the display is plotted.

The magnitude of the display is in dB below the peak jitter level in seconds. Frequency is on the x-axis. The right-most bin is the Nyquist frequency ($f_s/2$). This is a display of one spectral line.

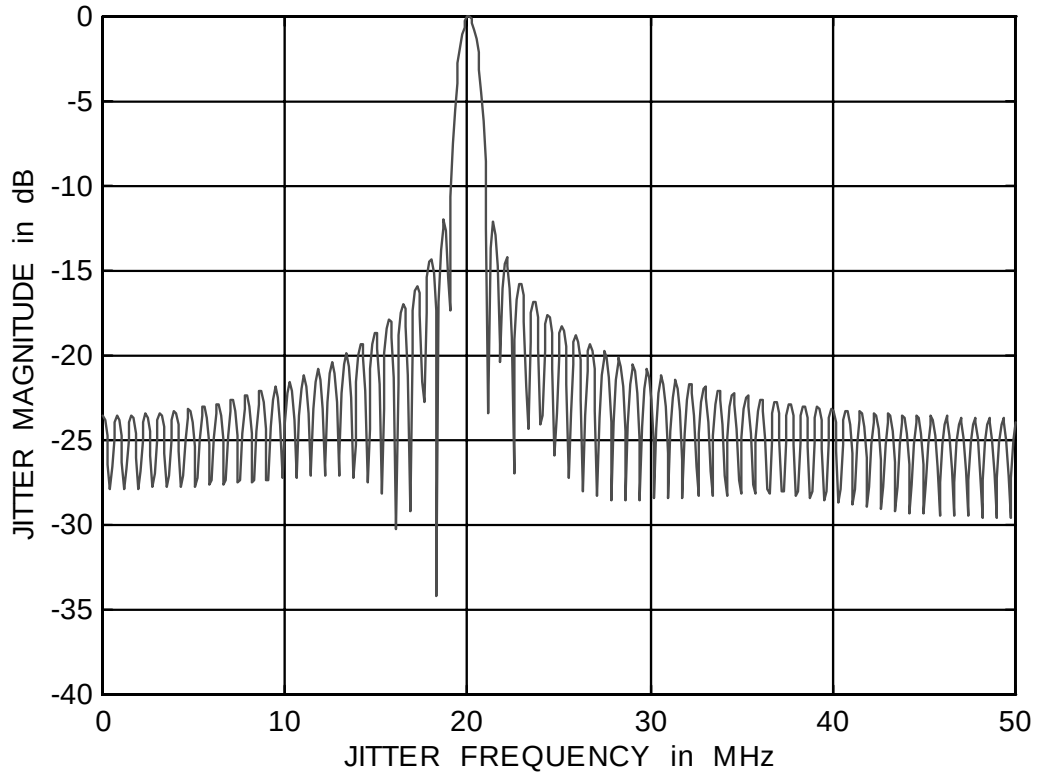
Jitter Spectrum

Nmax = 128 Nstep = 1

f_{clock} = 100 MHz f_s = 100 MHz
f_{pj1} = 20 MHz @ 0 dB

Kaiser-Bessel Window, alpha = 3
Padding Factor = 8

- **shows characteristic of Kaiser-Bessel window with alpha set to 3**



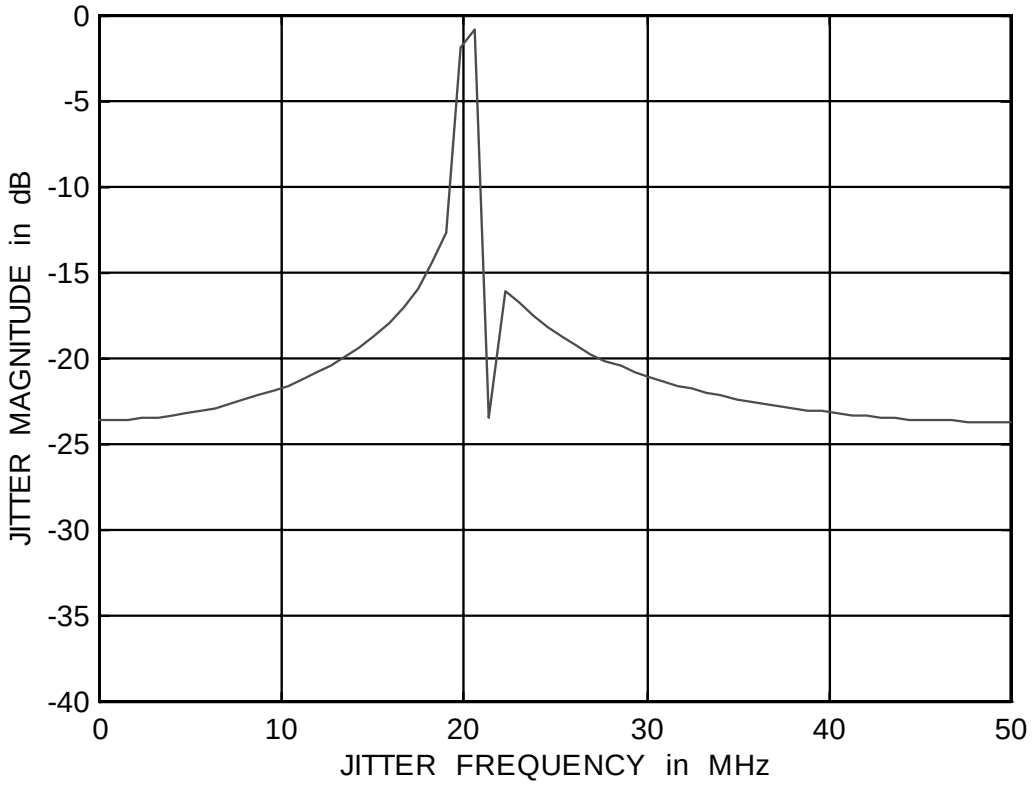
- **Display has good resolution, padding factor is large enough: a larger padding factor will require a larger data processing time**

Jitter Spectrum

Nmax = 128 Nstep = 1

f_{clock} = 100 MHz f_s = 100 MHz
f_{pj1} = 20 MHz @ 0 dB

Kaiser-Bessel Window, alpha = 3
Padding Factor = 1



- **Display has poor resolution, padding factor is too small.**

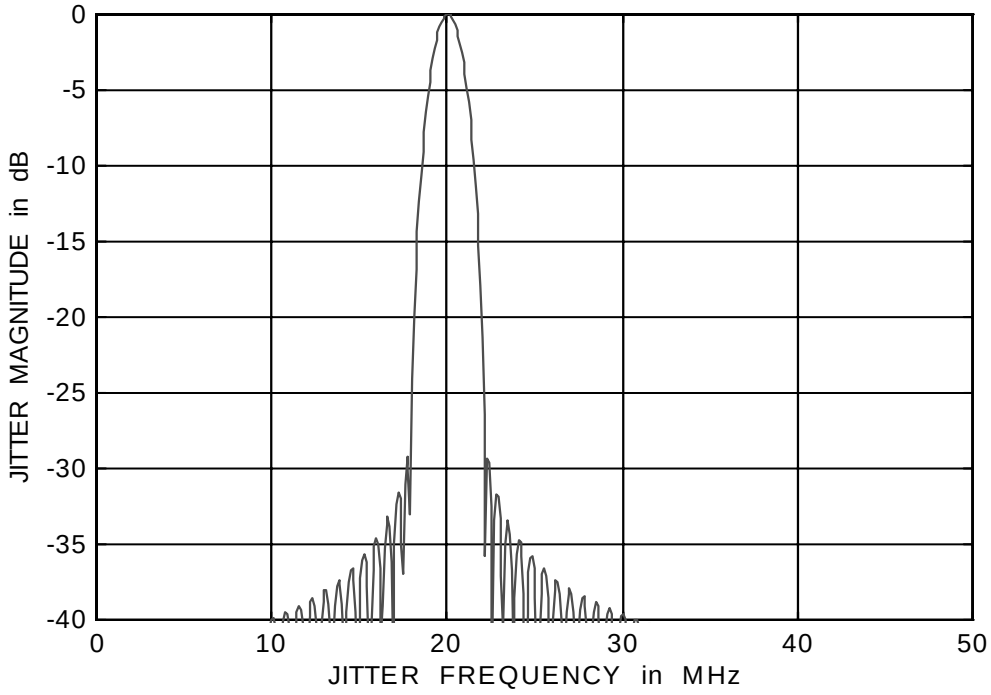
Jitter Spectrum

Nmax = 128 Nstep = 1

f_{clock} = 100 MHz f_s = 100 MHz
f_{pj1} = 20 MHz @ 0 dB

Kaiser-Bessel Window, alpha = 8
Padding Factor = 8

-shows characteristic of Kaiser-Bessel window with alpha set to 8



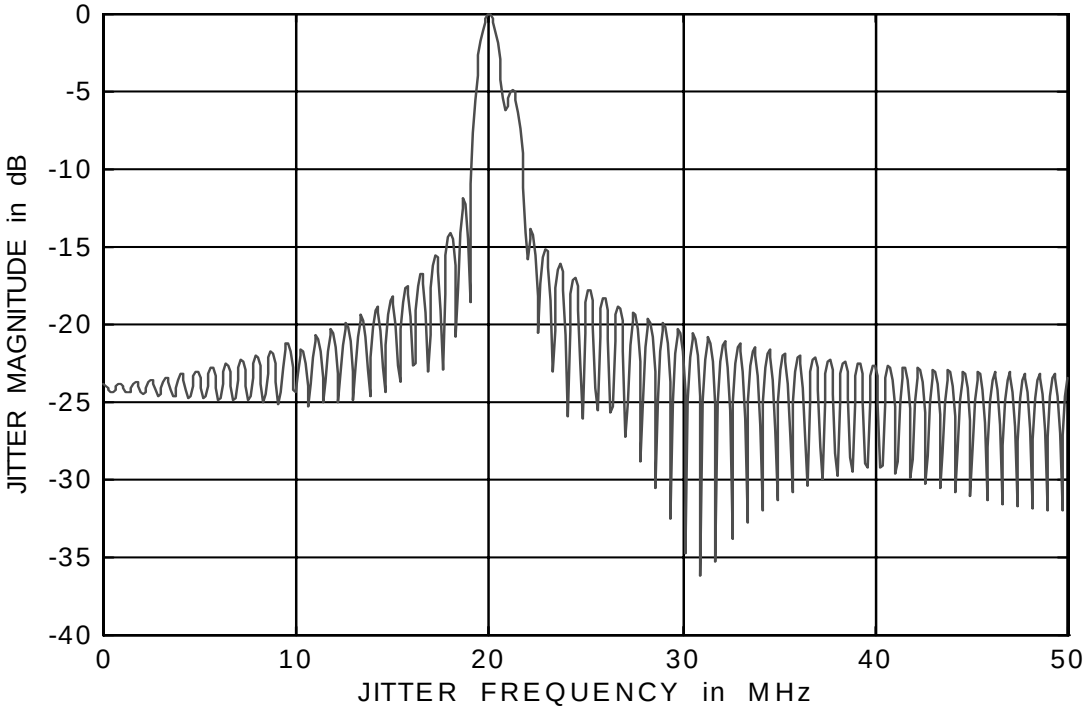
- **Note that with alpha set to 8 the central lobe is wider and the sidelobes are down more, compared with alpha set to 3**

Jitter Spectrum

Nmax = 128 Nstep = 1

f_{clock} = 100 MHz f_s = 100 MHz
f_{pj1} = 20 MHz @ 0 dB
f_{pj2} = 21 MHz @ -5 dB
f_{pj3} = 10 MHz @ -30 dB

Kaiser-Bessel Window, alpha = 3
Padding Factor = 8



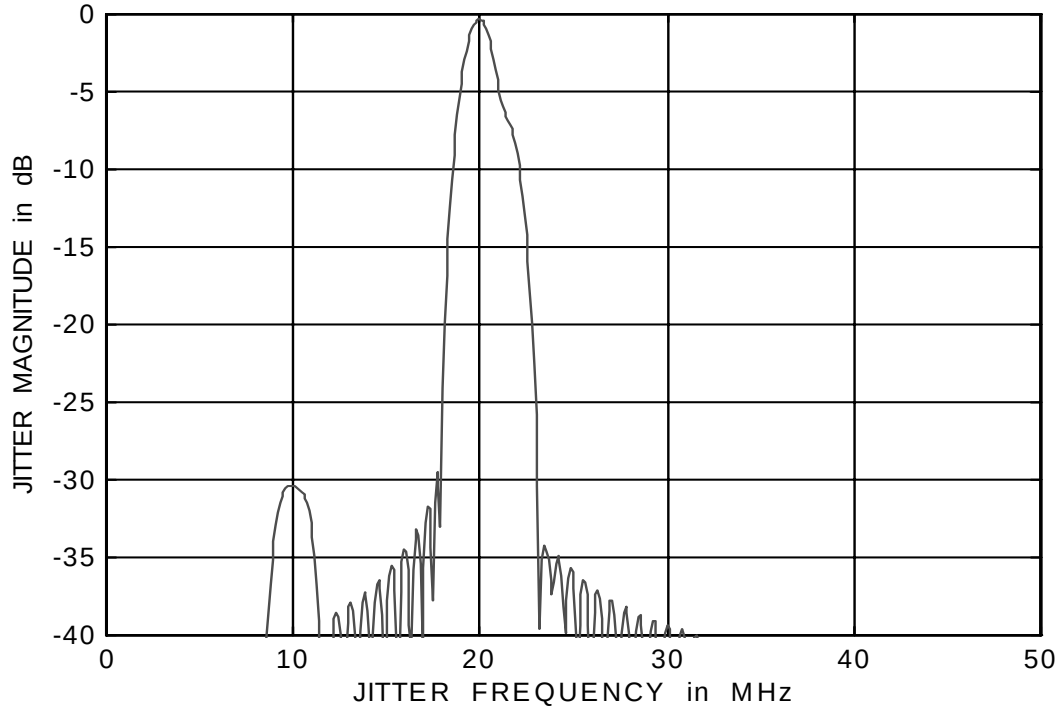
- **The 20 MHz and 21 MHz jitter components are resolved and the 10 MHz component is not seen with alpha set to 3.**

Jitter Spectrum

Nmax = 128 Nstep = 1

f_{clock} = 100 MHz f_s = 100 MHz
f_{pj1} = 20 MHz @ 0 dB
f_{pj2} = 21 MHz @ -5 dB
f_{pj3} = 10 MHz @ -30 dB

Kaiser-Bessel Window, alpha = 8
Padding Factor = 8



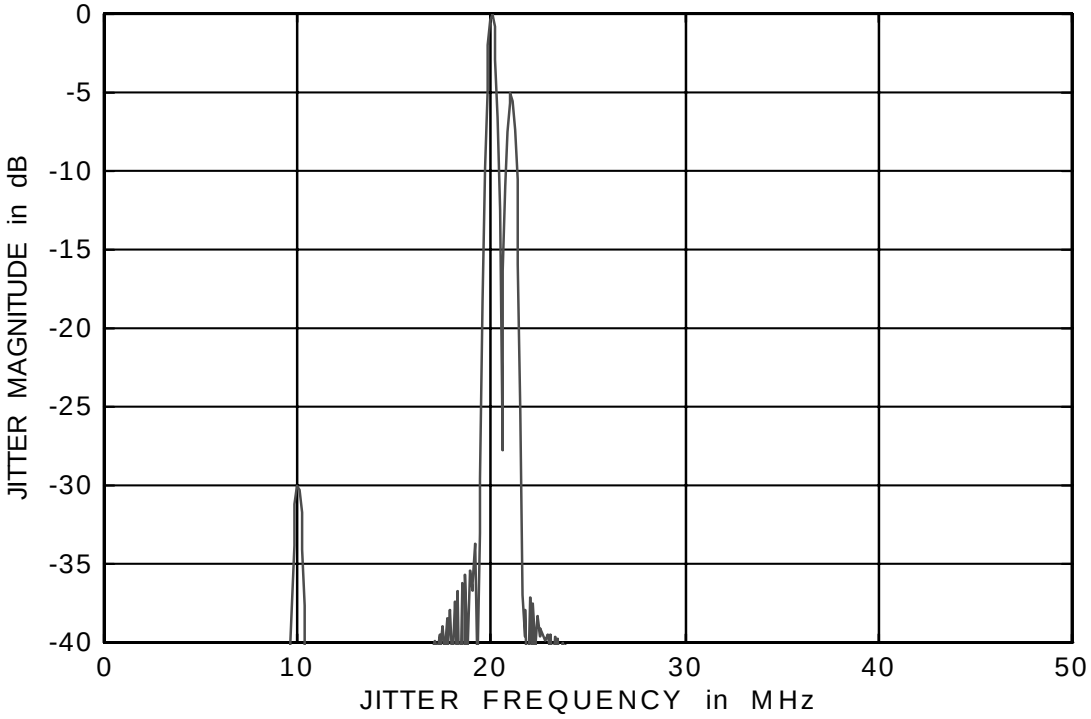
- **The 20 MHz and 21 MHz jitter components are not resolved and the 10 MHz component is seen with alpha set to 8**

Jitter Spectrum

Nmax = 512 Nstep = 1

f_{clock} = 100 MHz f_s = 100 MHz
f_{pj1} = 20 MHz @ 0 dB
f_{pj2} = 21 MHz @ -5 dB
f_{pj3} = 10 MHz @ -30 dB

Kaiser-Bessel Window, alpha = 8
Padding Factor = 2



- **All jitter components are resolved. Nmax is large enough, at the cost of increased measurement and data processing time.**

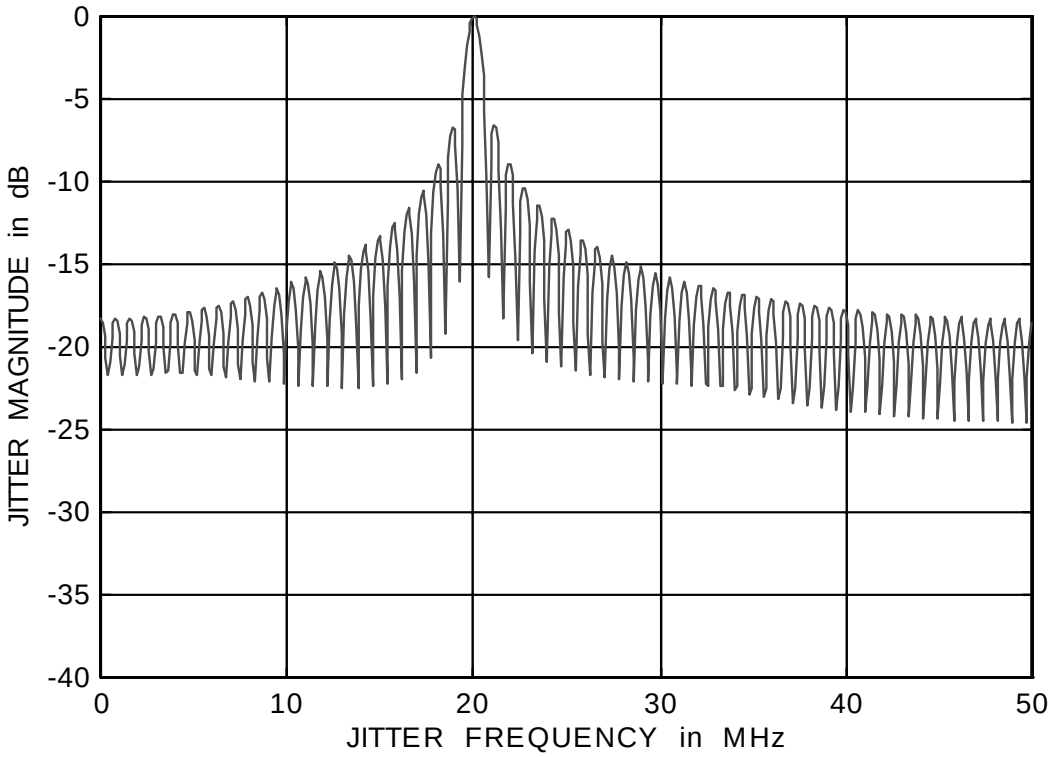
Jitter Spectrum

Nmax = 128 Nstep = 1

f_{clock} = 100 MHz f_s = 100 MHz
f_{pj1} = 20 MHz @ 0 dB

Rectangular Window
Padding Factor = 8

- **shows characteristic of Rectangular window; main sidelobes down ~ 7 dB**



- **This window has a constant magnitude as a function of N, this is like having no window.**

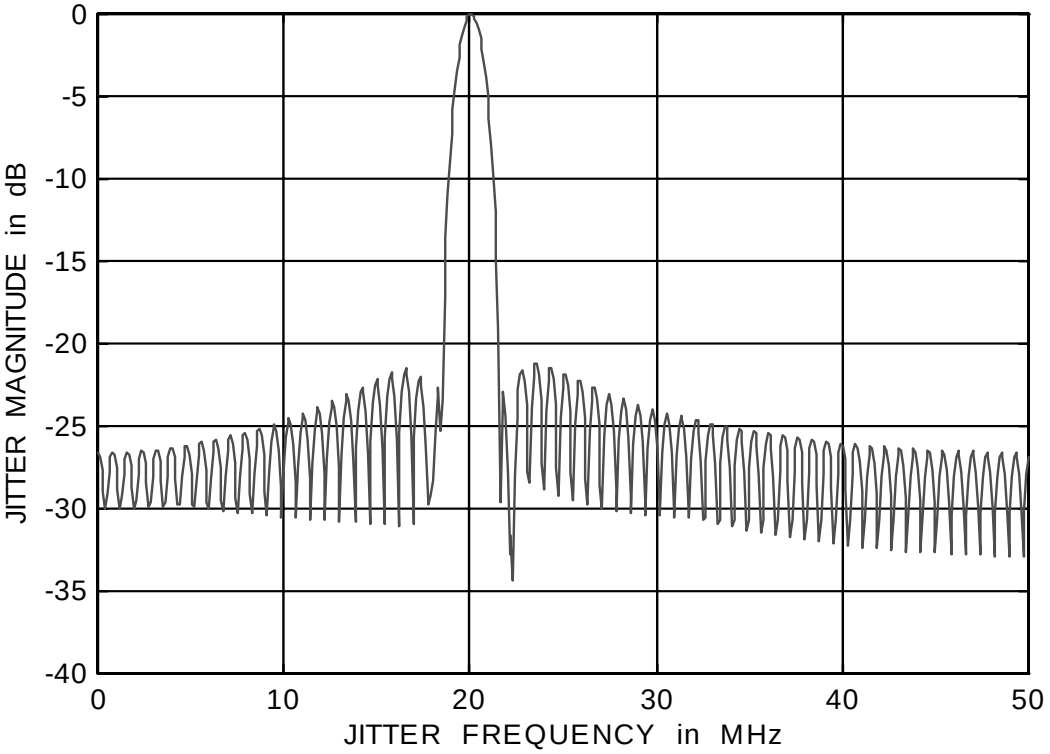
Jitter Spectrum

Nmax = 128 Nstep = 1

f_{clock} = 100 MHz f_s = 100 MHz
f_{pj1} = 20 MHz @ 0 dB

Hamming Window
Padding Factor = 8

- **shows characteristic of Hamming window; main sidelobes down ~ 22 dB**



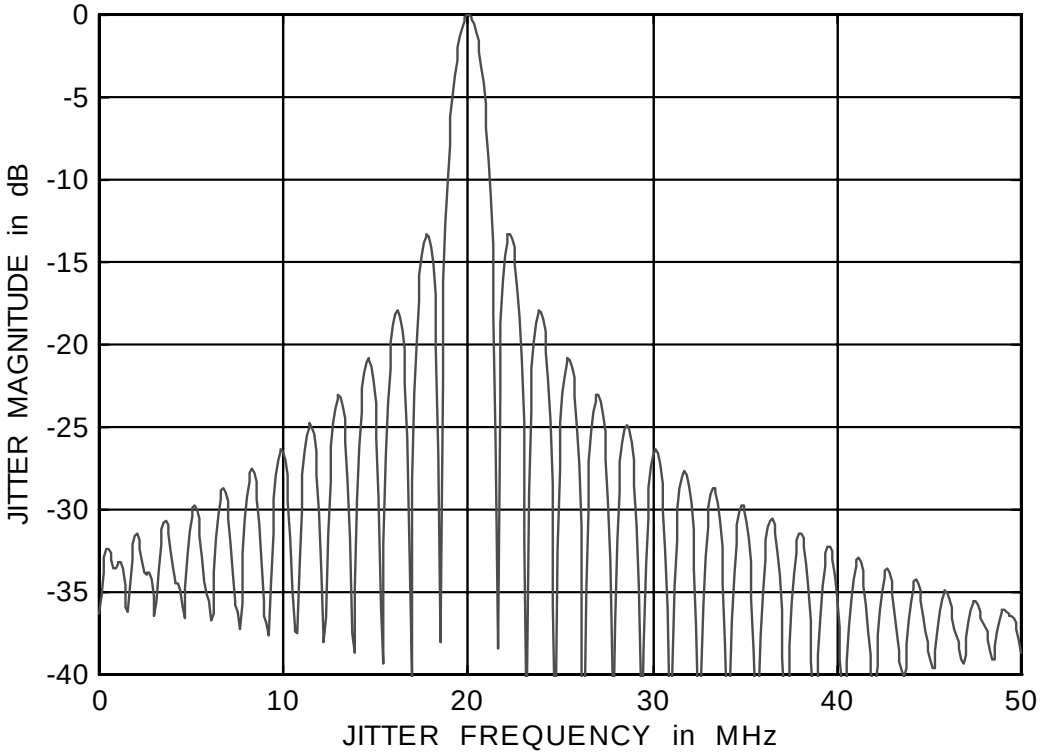
Jitter Spectrum

Nmax = 128 Nstep = 1

f_{clock} = 100 MHz f_s = 100 MHz
f_{pj1} = 20 MHz @ 0 dB

Triangular Window
Padding Factor = 8

-shows characteristic of Triangular window; main sidelobes down ~ 14 dB



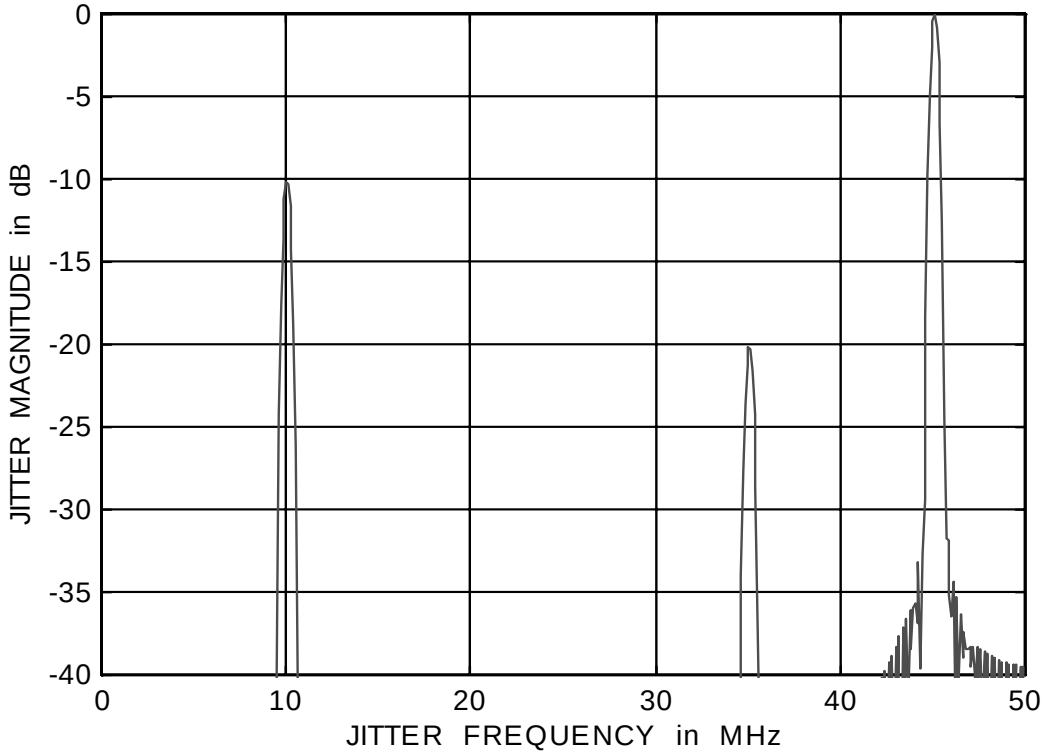
-The triangular window was used in an example earlier in this paper

Jitter Spectrum

Nmax = 512 Nstep = 1

f_{clock} = 100 MHz f_s = 100 MHz
f_{pj1} = 45 MHz @ 0 dB
f_{pj2} = 90 MHz @ -10 dB
f_{pj3} = 135 MHz @ -20 dB

Kaiser-Bessel Window, alpha = 8
Padding Factor = 2



- **The 45MHz jitter is at 45MHz. The 90MHz jitter is aliased to 10MHz. The 135MHz jitter is aliased to 35MHz.**

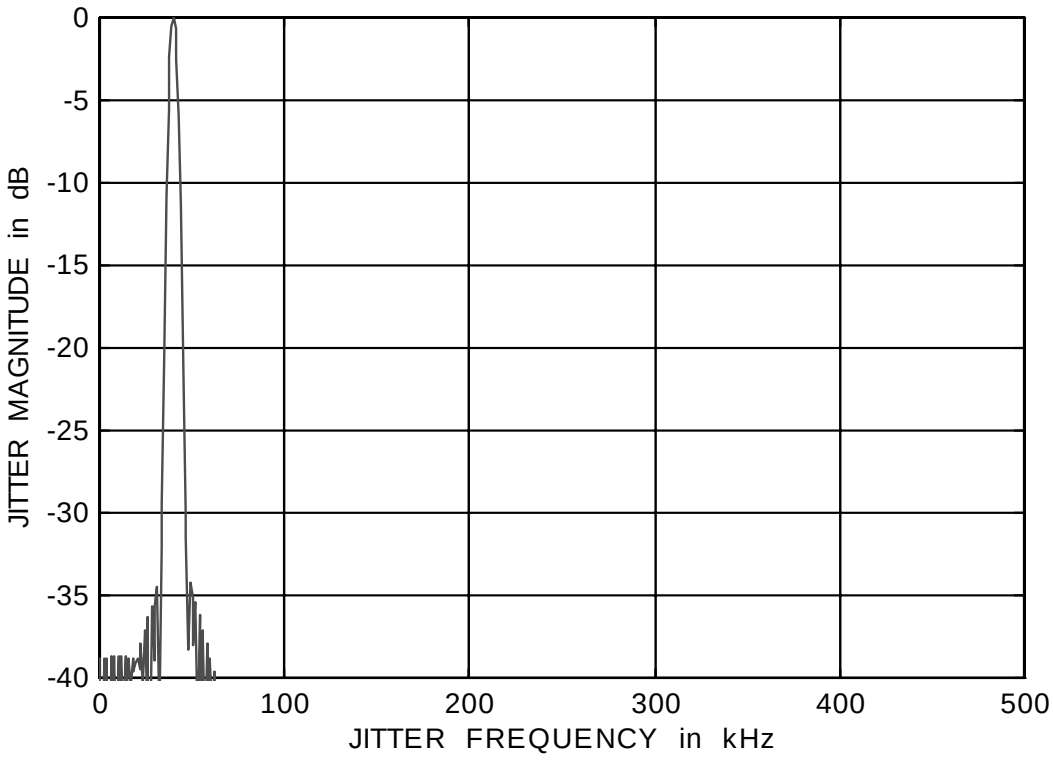
Jitter Spectrum

Nmax = 51 200 Nstep = 100

f_{clock} = 100 MHz f_s = 1 MHz
f_{pj1} = 40 kHz @ 0 dB

Kaiser-Bessel Window, alpha = 8
Padding Factor = 2

- **This setting of Nstep allows the display of low frequency jitter and saves data acquisition time and data processing time. Watch out for aliasing.**



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APPENDIX D

Investigating switcher phase noise on 622 Mbit/s ATM PLL device

Test Setup

This section goes through an application demonstration searching for phase noise jitter caused by asynchronous interference, such as power supply switcher noise, using WAVECREST's DTS-2070C. This jitter source can cause crystal references, and PLL's driven by these references, to jitter at the period of the interference.

In many cases, the phase noise measured at the oscillator output is related to the noise rejection specifications of the devices' power supply circuit.

The following figures and illustrations show the test setup as well as the jitter identified, measured and displayed by WAVECREST's DTS-2070C and *Virtual Instrument* interface software.

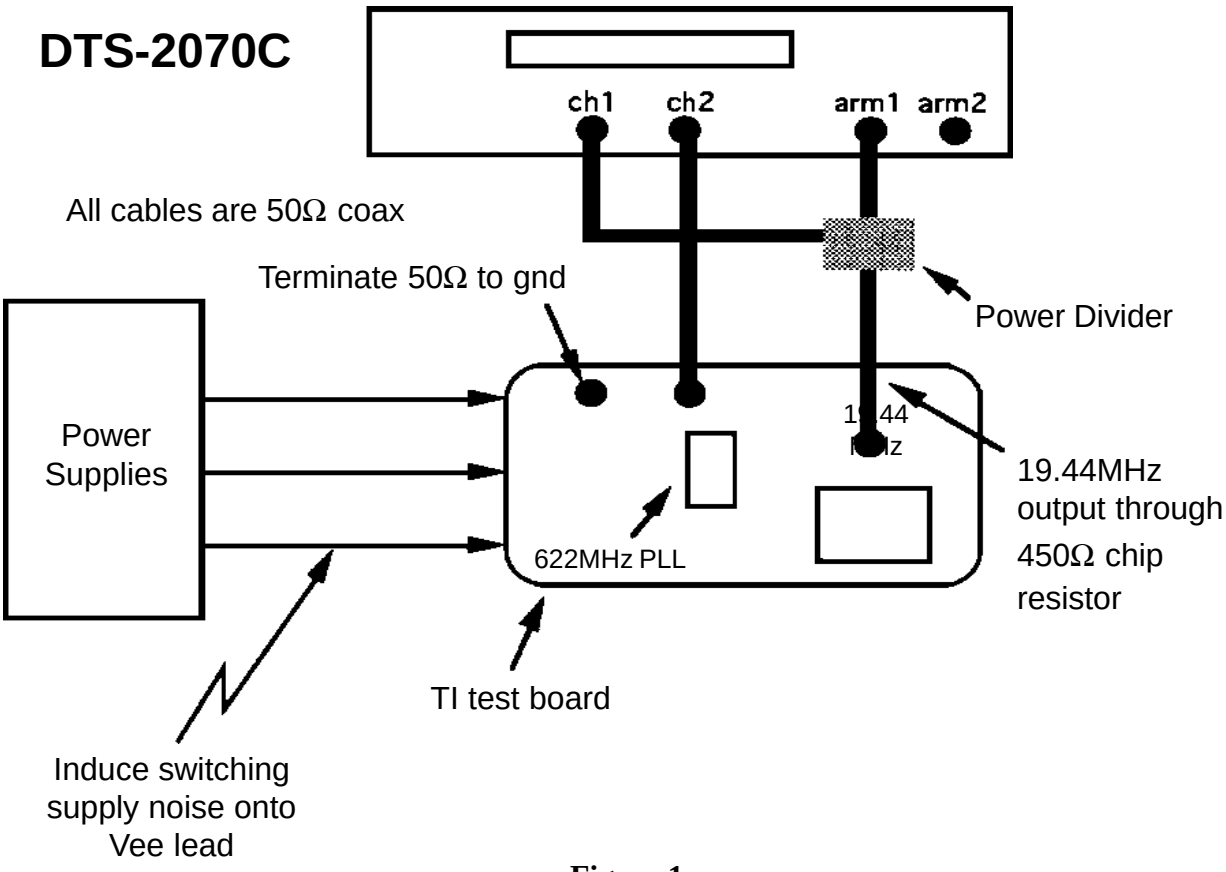

Figure 1

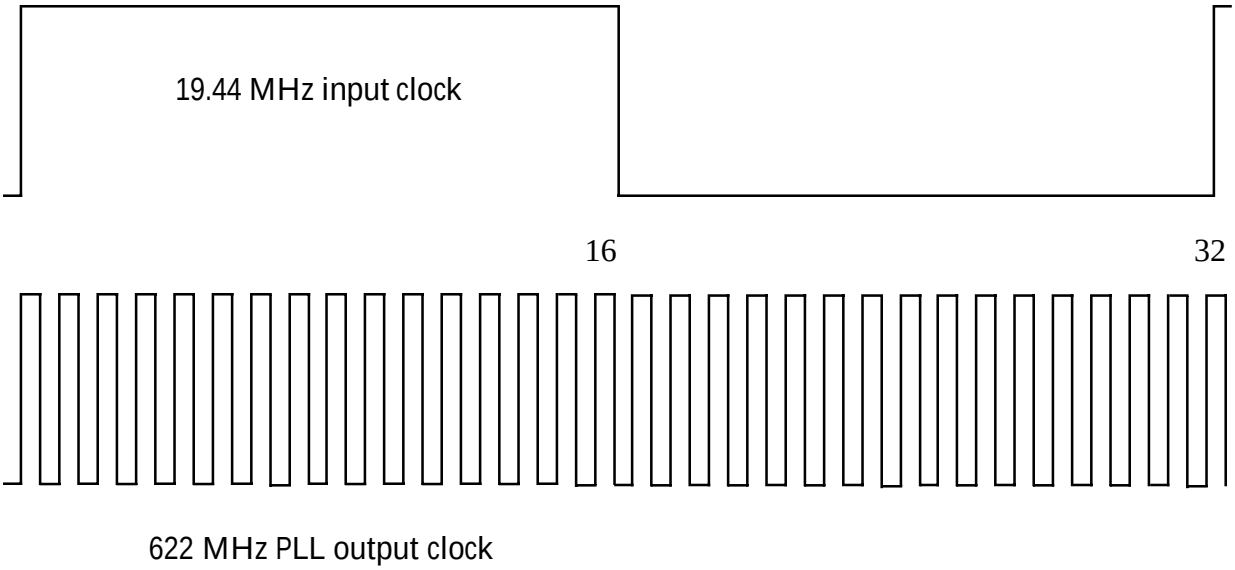

FIGURE 2

Figure 2 shows the count relationship of the 19.44 MHz input clock to the 622 MHz PLL output frequency. There are 32 outputs for every input cycle of the 19.44 MHz clock. In the following graphs the distortion of several of these cycles as a function of their placement with respect with in the input clock is illustrated.

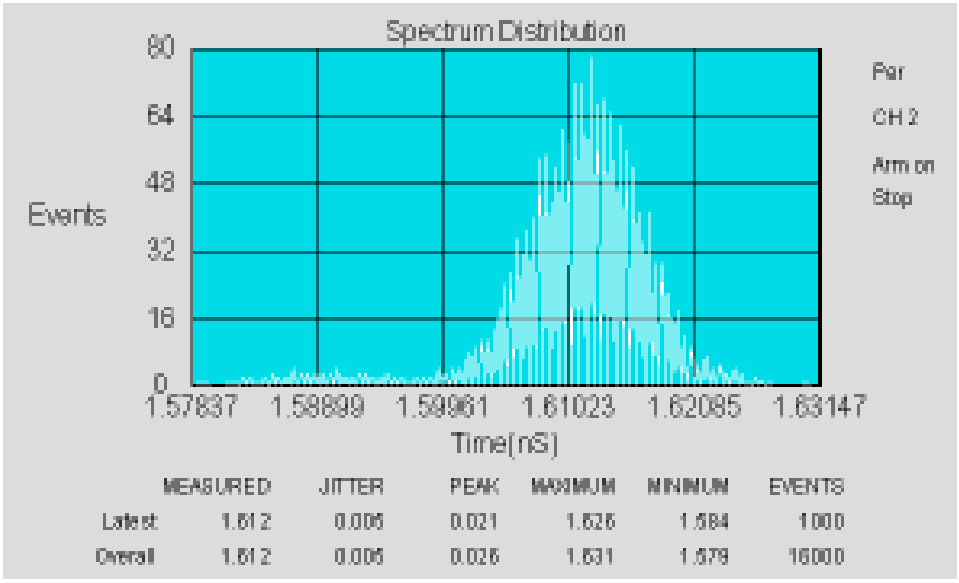

FIGURE 3

The first indication of a problem can be seen in Figure 3. The 622MHz output histogram shows offset short cycles down to 1.579ns.

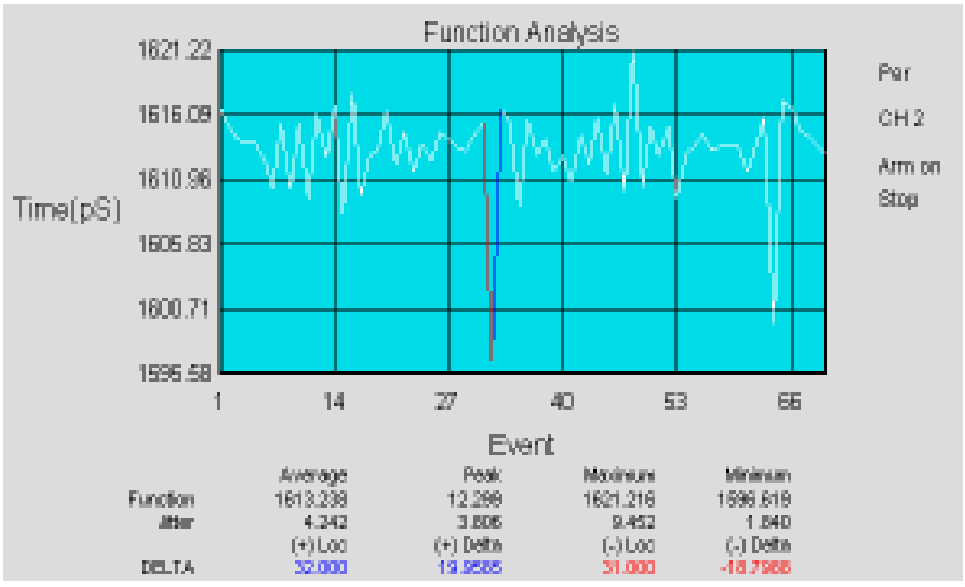

FIGURE 4

Looking at the same output pin of the device with the DTS' *VIRTUAL INSTRUMENT* Function Analysis window we can see that the output cycle directly adjacent to the falling edge of the input (the 32nd cycle) is short. The Function Analysis window is displaying the cycle-cycle output of
the DUT.

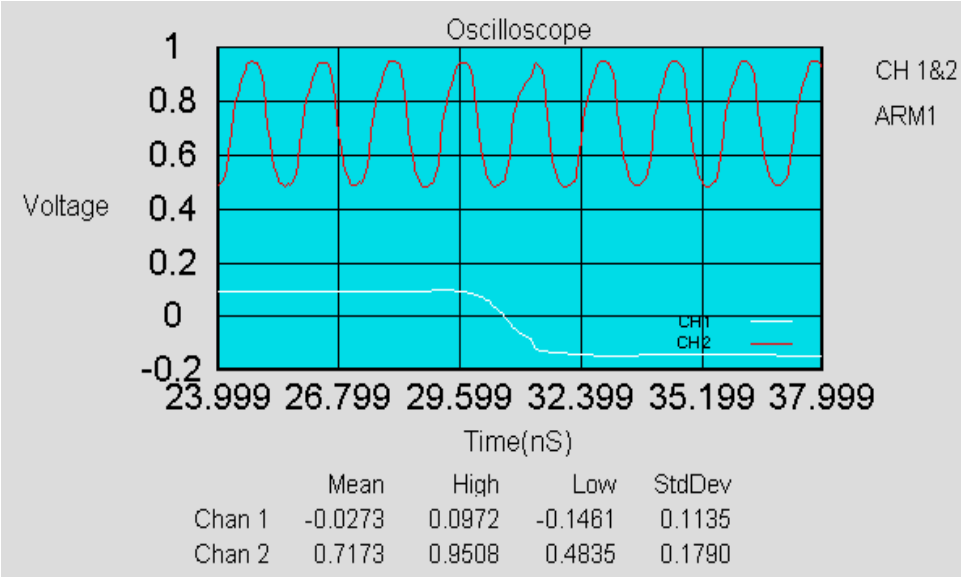

FIGURE 5

Using the Oscilloscope window on the DTS the user can digitize the waveforms on both channels. In figure 5, see the slight rise time distortion on channel 2 corresponding to the falling edge on channel 1. That slight distortion is causing the short cycle caught by the Function Analysis window.

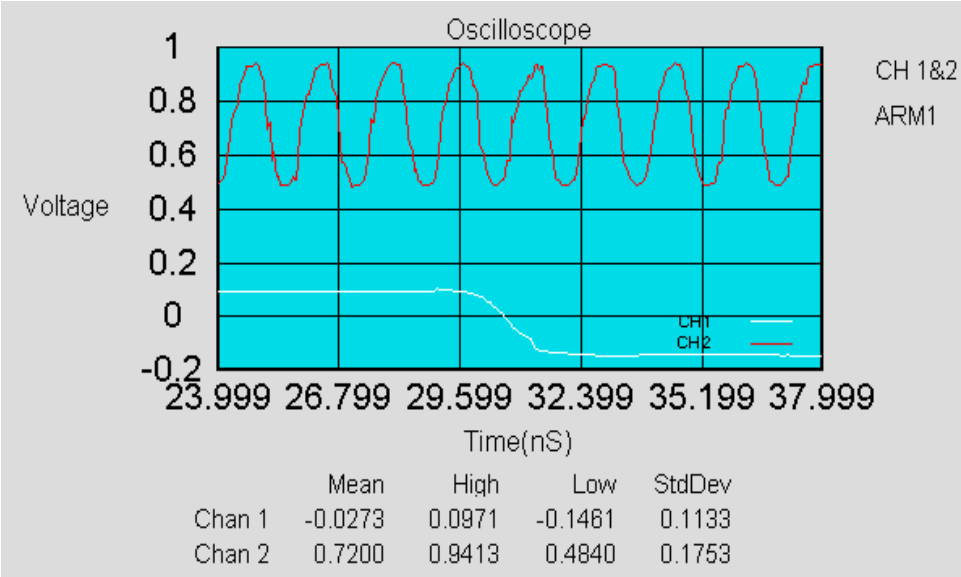

FIGURE 6

In Figure 6, the 130 kHz jitter on the input clock is showing up on channel 2 as a fuzzy trace when ever the VEE wire is placed near the switching power supply.

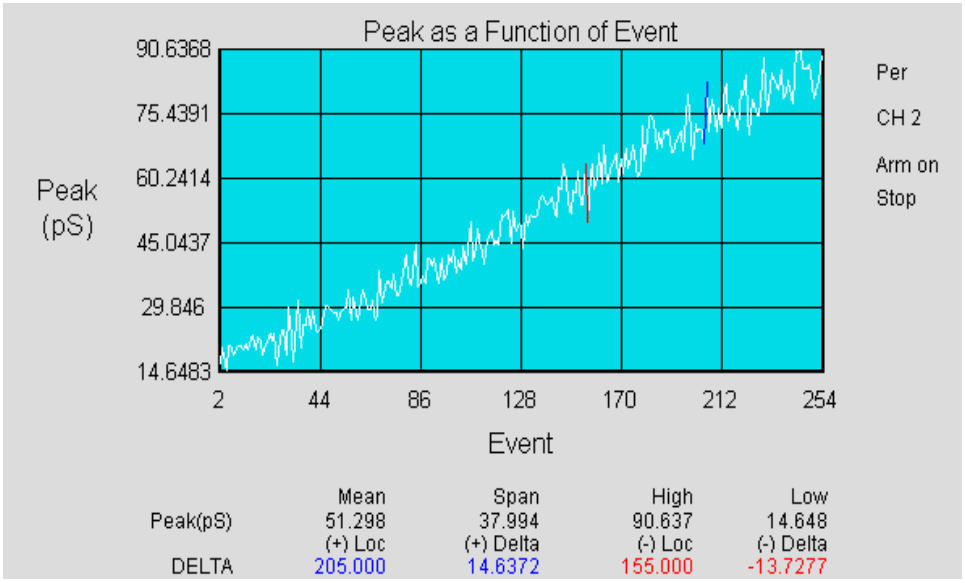

FIGURE 7

Further investigation of the output pin with the DTS' Jitter Analysis window showed that under some conditions the low frequency content of the phase noise of the 622 MHz output was higher than at other times. Compare figure 7 to Figure 8.

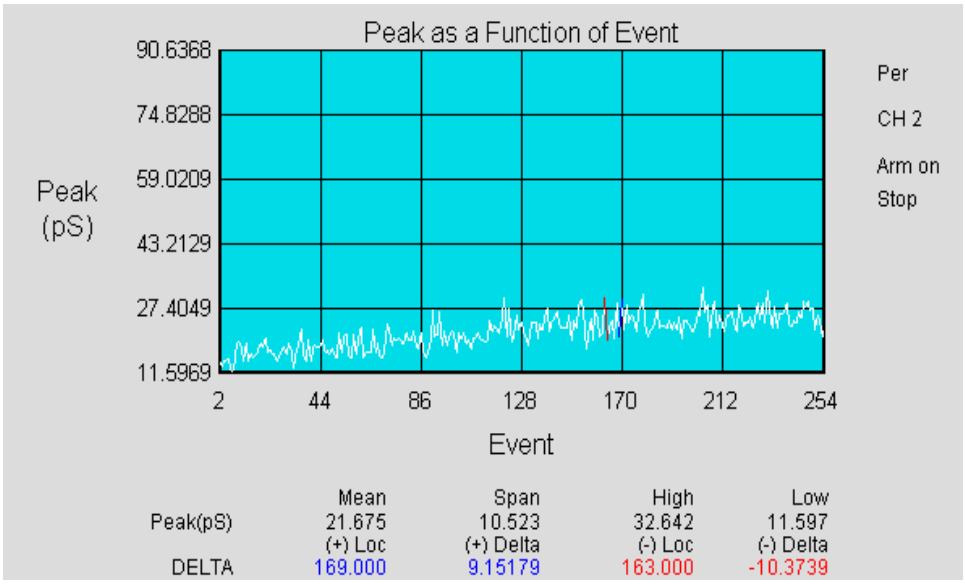

FIGURE 8

Figure 8 is showing much lower phase noise buildup than in Figure 7.

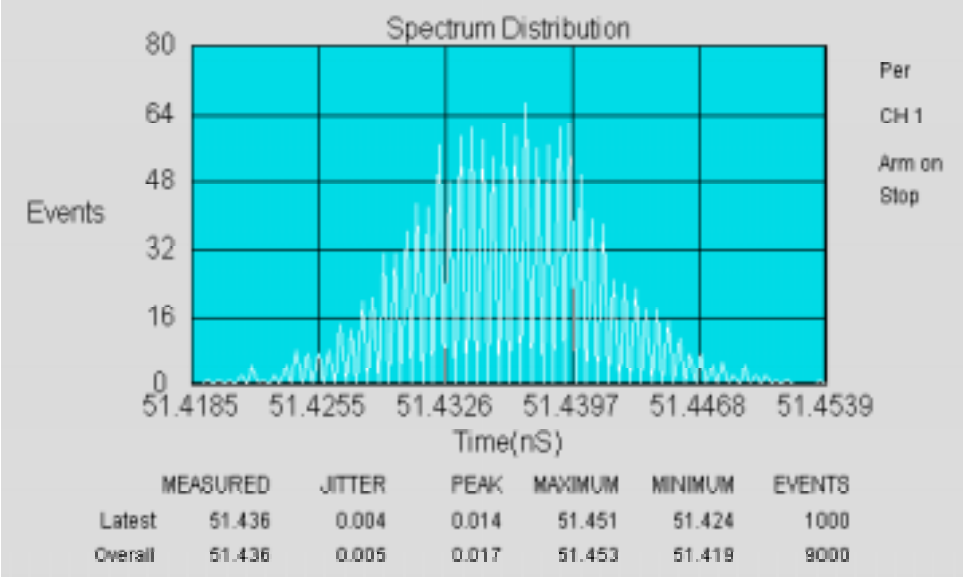

FIGURE 9

At first glance, Channel 1, which is the 19.44 MHz input, looks very nice with a low jitter rms value of 5ps.

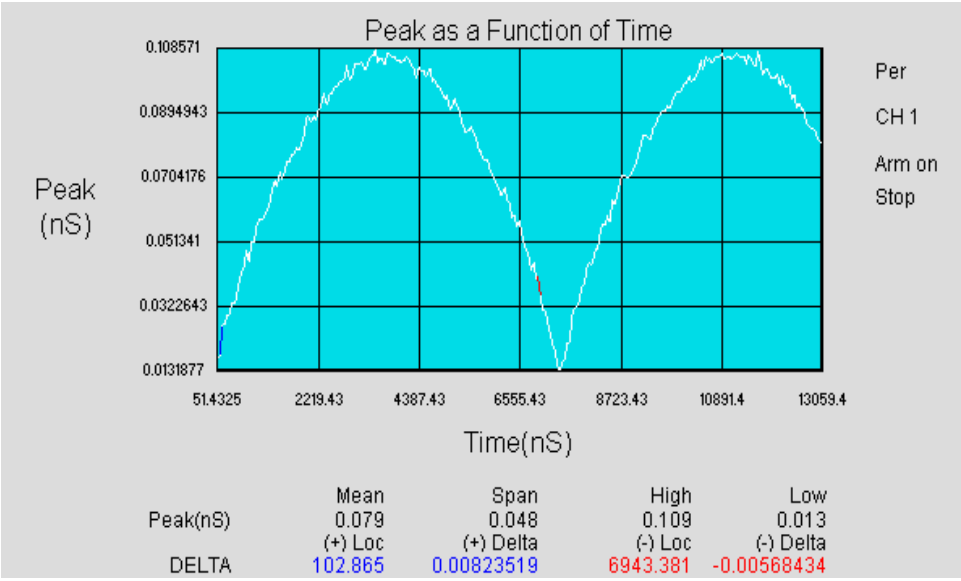

FIGURE 10

Using Jitter Analysis to look for low frequency phase noise showed an interfering signal riding on the input clock. The period of the interference was 7.7 microseconds. This corresponds to 130 kHz, which is the frequency of the switching power supply used to power this test demo.

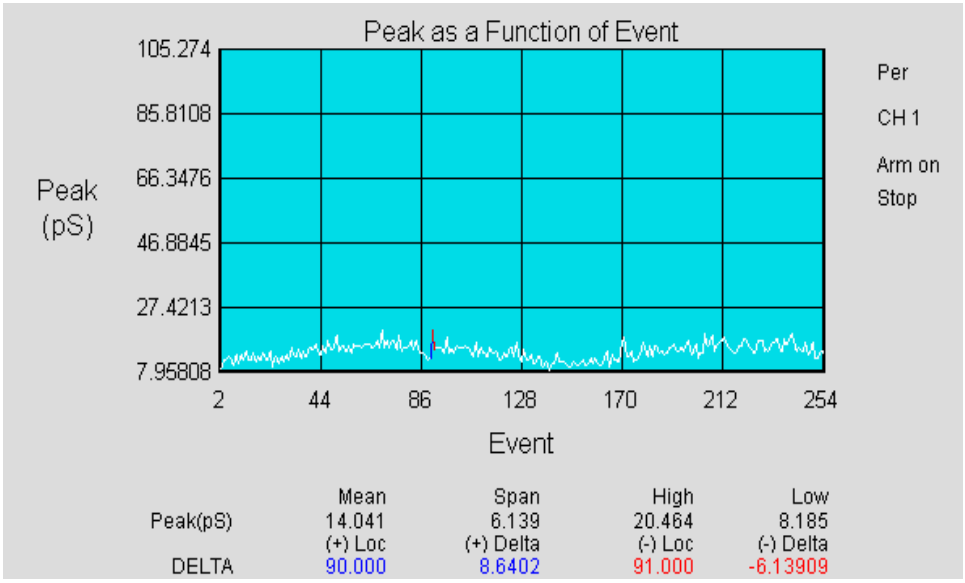

FIGURE 11

Whenever the VEE wire was placed near the power supply box, the jitter would increase. When the wire was moved away, the jitter would decrease. This corresponds to variations seen in Figures 5 and 6 as well. It would seem that the oscillator used to supply a reference to the PLL was causing the PLL to go out of specification.

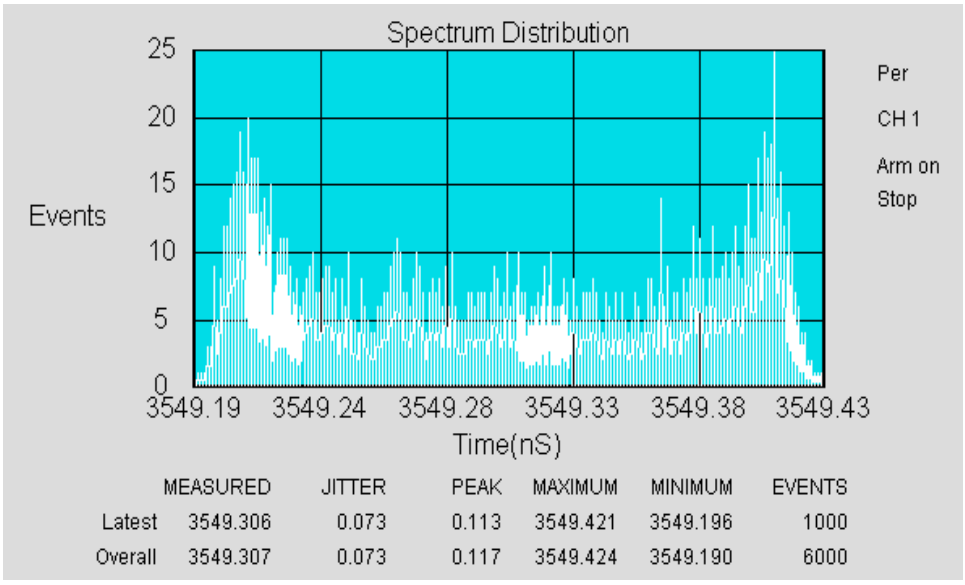

FIGURE 12

Using the Spectrum window the user can take a look at the histogram for the jitter on Channel 1 by setting the stop count on the DTS to where the peak jitter occurs, 70 cycles. Compare this with the display in Figure 9 which was looking for single-cycle jitter.

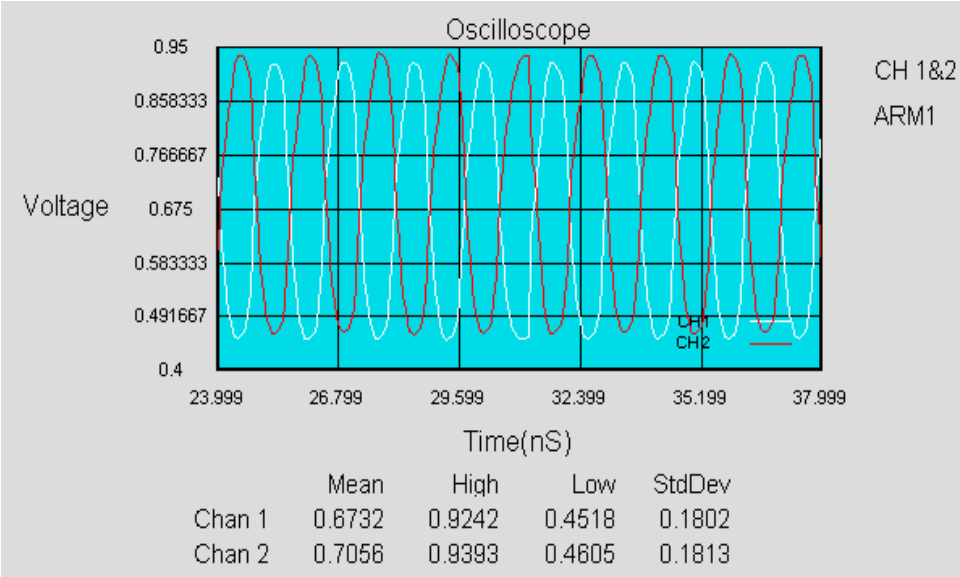

FIGURE 13

In Figure 13, the test setup was changed and Channel 1was connected to the complementary output of Channel 2 to look at the differential charateristics of the PLL.

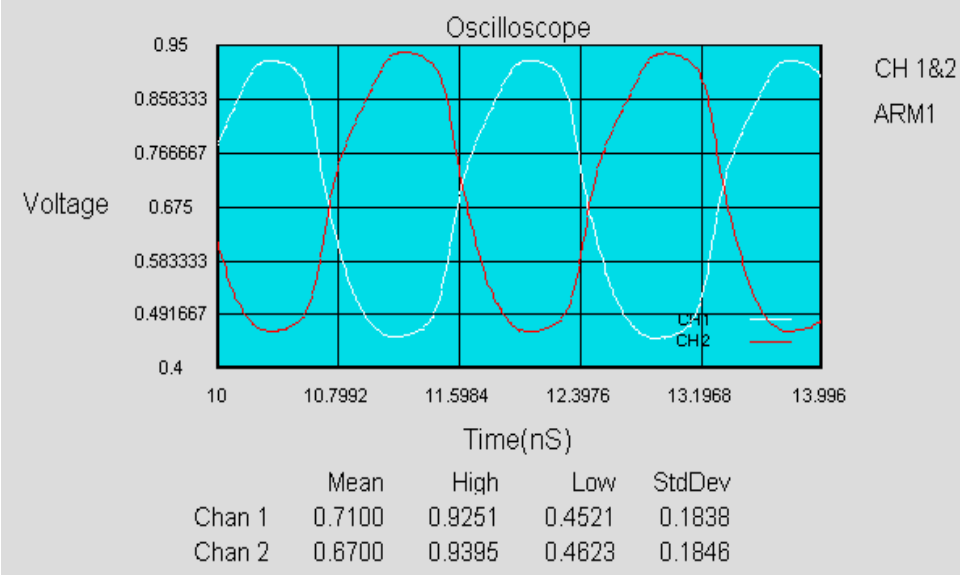

FIGURE 14

In Figure 14, the digitized window scaling has been adjusted for a closer view of the two signals.

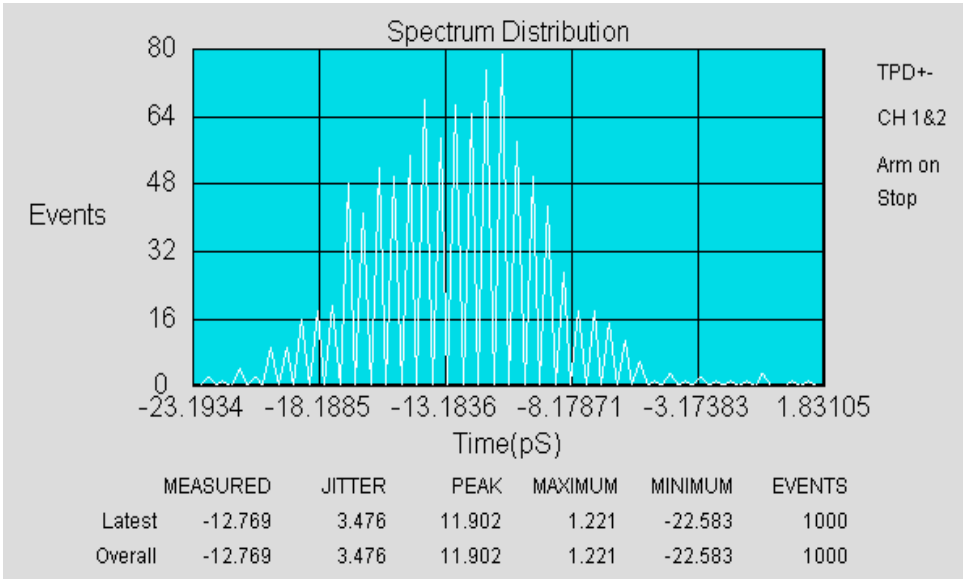

FIGURE 15

In Figure 15, the DTS is measuring the TPD+- at the complementary outputs. Notice the low jitter.

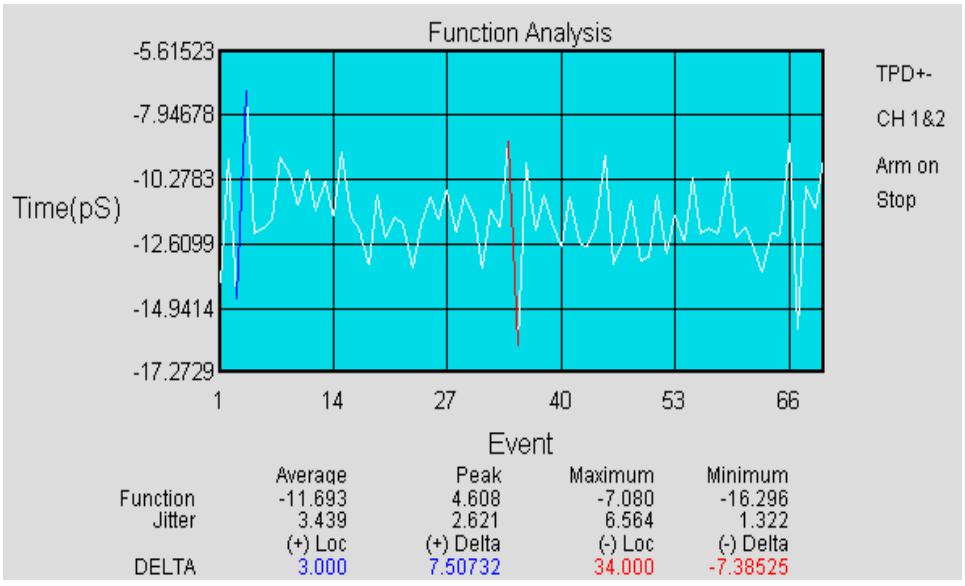

FIGURE 16

The Function Analysis window in *Virtual Instrument* enables the user to observe the 622MHz cycle-to-cycle crossing delay variations of each output and to detect anomalies.

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APPENDIX E - Jitter Definition and Related Terminologies

1) Jitter
2) Correlated (deterministic/systematic) Jitter
3) Non-Correlated (Random) Jitter
4) Period Jitter
5) Cycle to Cycle Jitter
6) Long Term (Accumulated) Jitter
7) Low Frequency Jitter (Wander)
8) High Frequency Jitter
9) Jitter Spectrum
10) Input to Output Jitter
11) Jitter Tolerance (Receiver)
12) Jitter Generation (Transmitter)
13) Jitter Transfer (Transmitter/Receiver)
14) Data Dependent Jitter
15) Duty Cycle Distortion Jitter
16) Inter-symbol Interference (ISI)
17) Bit Error Ratio (BER)
18) Eye Diagram

Definitions

1) Jitter

High frequency deviation from the ideal timing of an event. Jitter is a period/frequency displacement of a signal from its ideal location. These displacements can occur in amplitude, phase, and pulse width and are generally categorized as either deterministic or random.

2) Correlated (deterministic/systematic) Jitter

Sum of Duty Cycle Distortion (DCD) and Data Dependent Jitter (DDJ). Jitter is based on real and repeatable direct measurements. Deterministic jitter itself may be broken into two major components - those based on the accuracy of the duty cycle of the information and those based on interaction of the 1's and 0's due to the limited bandwidth of the transmission system.

Deterministic jitter are those timing variations that are repeatable within a system and whose cause can generally be directly attributable to specific physical components or events. An example of this would be the jitter caused by the frequency selective attenuation and phase delay of a signal in a transmission line.

3) Non-Correlated (Random) Jitter

The probabilistic jitter created by random or Gaussian noise effects (shot, thermal, 1/f, etc.). Random jitter components are *rms* summed together. The ratio of peak-to-peak to rms equivalent random jitter is a factor determined by Gaussian probability of error, that is, the desired bit-error ratio. For example:

BER = 2.5E-10

Random jitter is that portion of jitter that is not repetitive in nature and is caused by external or internal noise in a system (thermal noise, EMI, etc.) This jitter is not directly predictable. It is measured by using a data pattern free of DDJ (i.e., the same pattern used to measure DCD) relative to the transmitter clock. Averaging is turned off, but infinite persistence is enabled.

4) Period Jitter

Variation in the output clock period. Important because it causes short clock cycles that reduce timing margins in synchronous circuits such as processors, reference to PLL, the period jitter is the worst case period deviation from ideal that will ever occur on the output of the PLL. The period jitter will represent an upper bound to the cycle to cycle jitter.

5) Cycle to Cycle Jitter

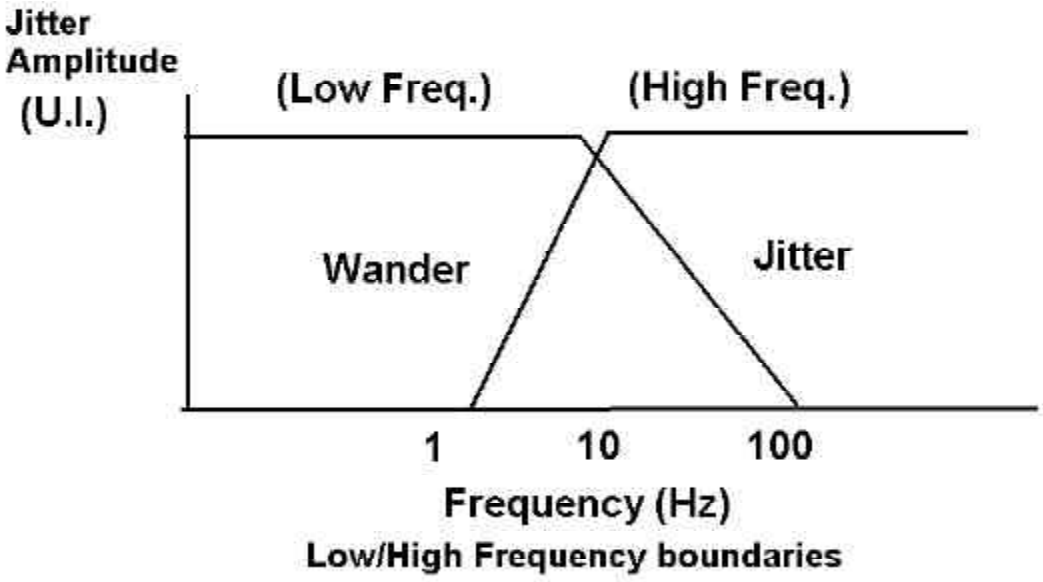
The deviation between periods of two adjacent cycles, i.e. variation of period N relative to period N-1. Because cycle to cycle jitter is defined as two adjacent periods this number is typically the smallest jitter that can be specified.

6) Long term (Accumulated) Jitter

The displacement of clock edges relative to an ideal clock over more than one cycle.

7) Low Frequency Jitter (Wander)

Jitter induced by frequency modulation below 10Hz.



Low/High Frequency boundaries

8) High Frequency Jitter

Jitter induced by frequency modulation above 10Hz.

9) Jitter Spectrum

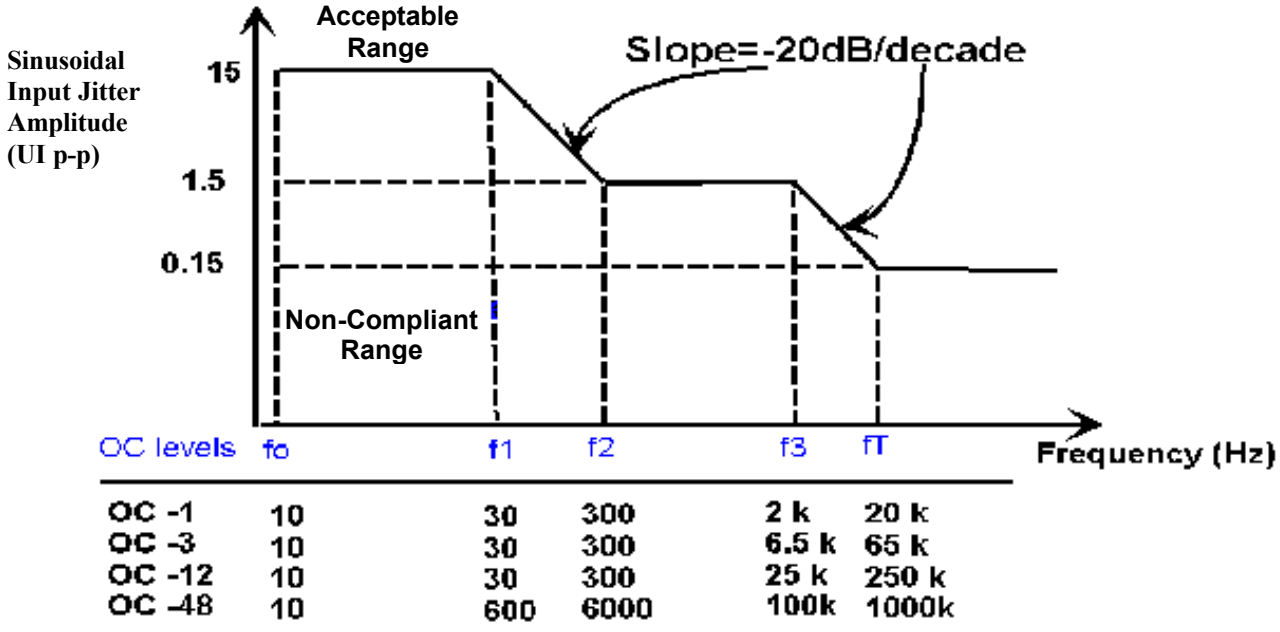
A FFT spectrum representation of Time Domain data which allows the frequency components of jitter to be displayed.

10) Input to Output Jitter

Variation in the delay from reference clock to output clock. Important when two more PLL clocks are cascaded in the system because it causes timing skew between the PLL clock outputs.

11) Jitter Tolerance

The amount of jitter that a receiver must accept and still recover data within a specified BER. Peak to peak time amplitude of sinusoidal jitter applied to the input data before output data pattern errors are observed in the recovered data. Expressed in Unit Interval peak to peak
(UIp-p), a UI is nominally one bit clock period.



SONET
Jitter Tolerance Limits

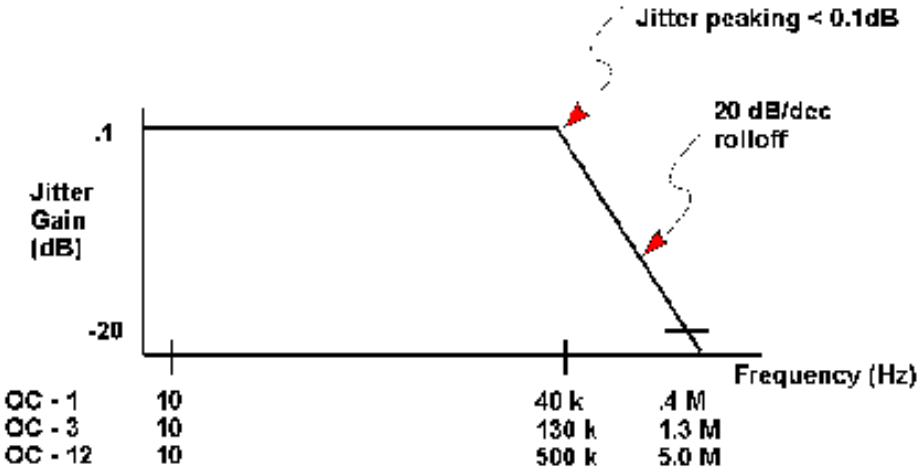
12) Jitter Generation

Generated jitter is caused by or added to a serial bit stream by a driver. Generated jitter measurements tell how much jitter is added to the data stream by sources such as inter-symbol interference, finite pulse width, pattern effects and clock-threshold offset. Described as a portion of Unit Interval (Ul) and limited to maximum 0.01 Ul for SONET using a 12kHz high pass filter. For common OC levels and data rates the following are SONET Jitter Generation Specifications.

OC level	Data Rate	Jitter Generation
OC-3	155 Mbits/sec	64ps
OC-12	622 Mbits/sec	16ps
OC-24	1.2 Gbits/sec	8ps
OC-48	2.4 Gbits/sec	4ps

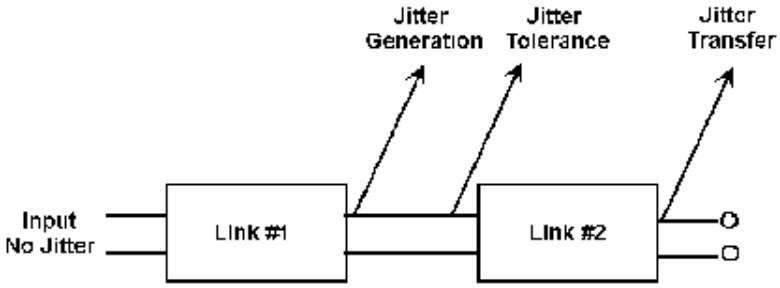
13) Jitter Transfer

Defined as the ratio of output data time jitter to the applied input data time jitter versus jitter frequency. Ratio is generally expressed in decibels [20 log (ratio)]



Jitter Transfer (SONET)
Bellcore GR-253-CORE

Jitter Accumulation



Random Jitter (RJ)

$$\text{Total Jitter} = \sqrt{(\text{Link \#1 jitter})^2 - (\text{Link \#2 jitter})^2}$$

Data Dependent Jitter (DDJ)

Total Jitter = Link #1 jitter Link #2 jitter

*DDJ increases linearly whereas RJ increases as root sum squared

14) Data Dependent Jitter

The time variation of data transition edges as caused by the length of time the prior state existed before changing states. This is from the subtle effects of saturation or cutoff time in electronic circuits. This effect contributes Intersymbol Interference, ISI, due to the attempt by prior bit to overlap into an adjacent bit interval, especially if the state interval approaches the state transition time.

DDJ is a measurement of intersymbol interference based on the maximum timing deviations caused by a worst-case data pattern. DDJ is affected by many environmental characteristics, in addition to the code used. These include the length of the cable, the integrity of the signal launched into the cable, and how well the cable is terminated.

15) Duty Cycle Distortion Jitter

Duty Cycle Distortion, or pulse-width distortion, is the difference in propagation delay time between the low-to-high and high-to-low delay times expressed in time units, or as a percentage of time relative to the original pulse duration time.

DCD manifests itself as either differences in the rise and fall times or differences in period for bits sent as a 0 compared to bits sent as a 1. DCD jitter alters the placement of all transitions in the data stream by about the same amount (in alternating directions), regardless of the bit pattern being sent. This is measured by sending a pattern down a communications link that does not exhibit DDJ and using an averaging mode on the oscilloscope to filter out any random jitter (RJ) that may be present.

16) Intersymbol Interference (ISI)

ISI is caused by short term storage effects in digital circuits. At any time, the received signal represents not only the current digital value but also the residues of previous digital values (determined by the system's impulse response). With random digital signals, the residuals appear on the eye diagram, rather like thermal noise. However, the levels are not random but are determined by the preceding digital pattern.

17) Bit Error Ratio (BER)

The bit error ratio, sometimes referred to as the bit error rate, is defined as the number of bits received in error divided by the total number of bits transmitted in a specified time interval. Within the specified interval, it is numerically equal to the bit error probability.

18) Eye Diagram

A method for assessing deterministic jitter. Typically obtained on an oscilloscope by writing all possible received sequences on top of each other while triggering the oscilloscope timebase from the data clock.

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